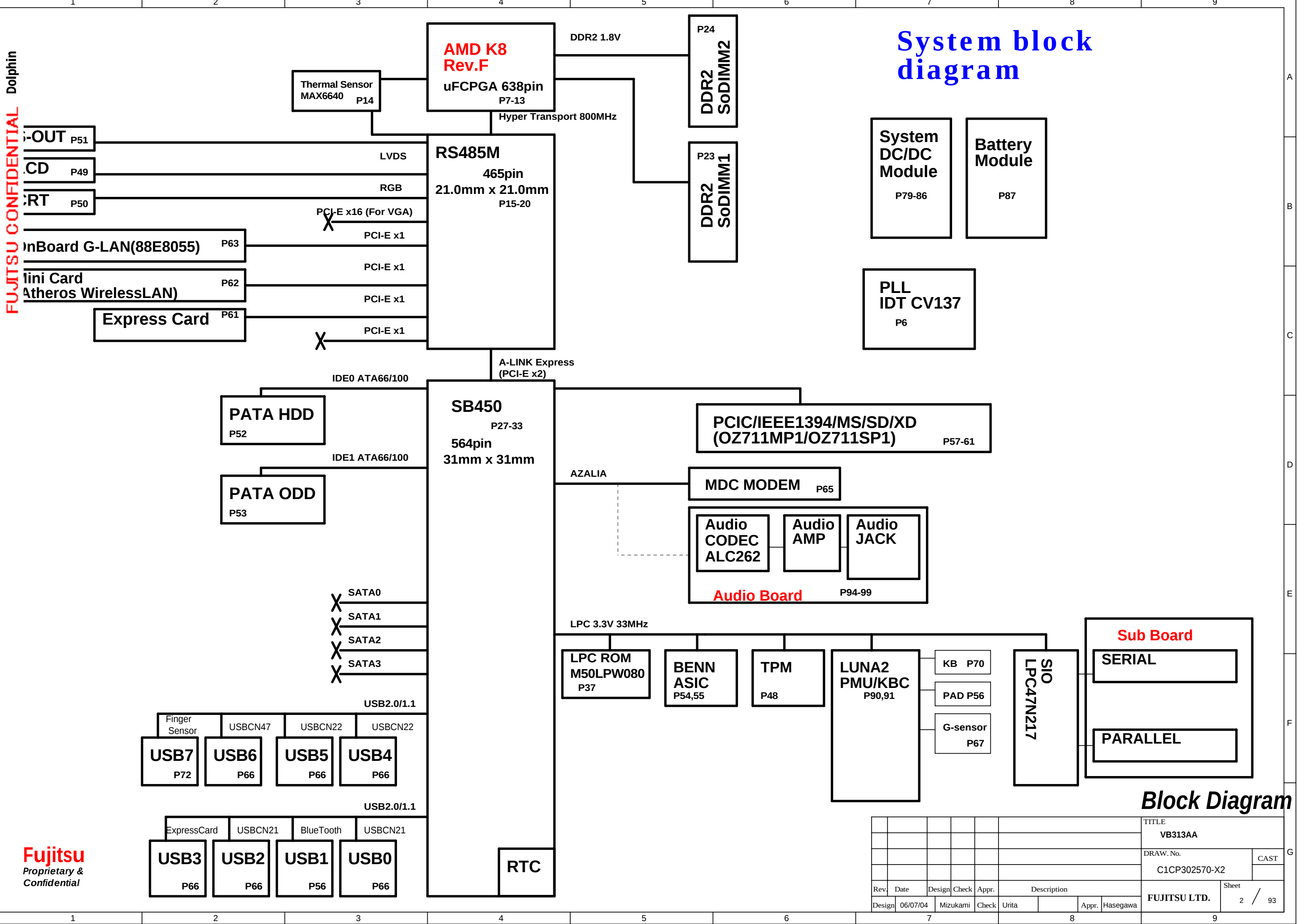
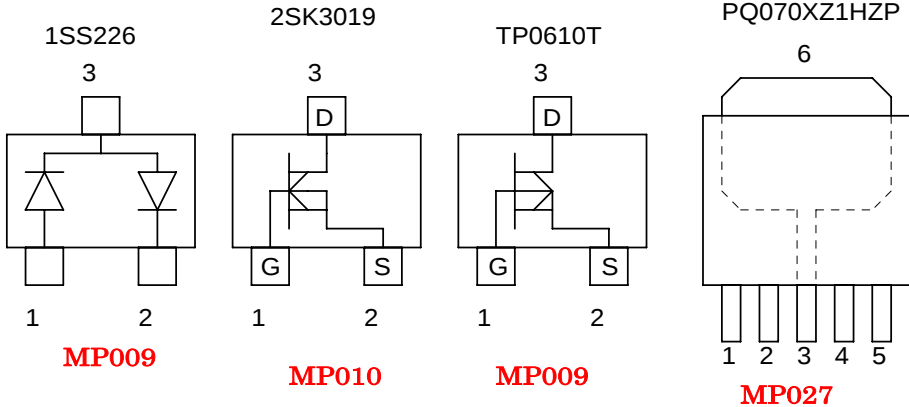
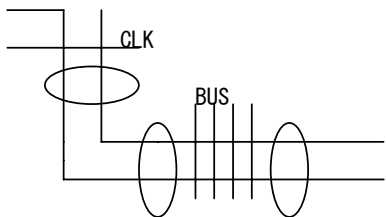
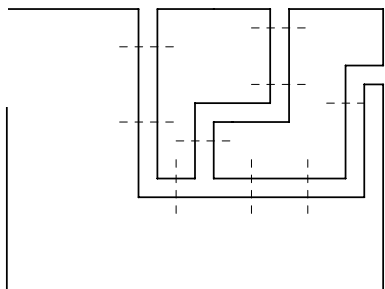


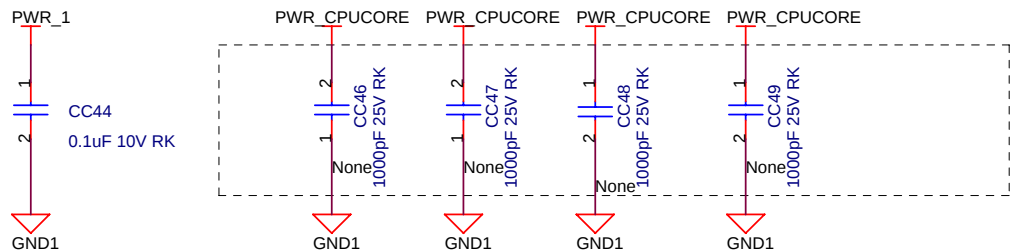


						TITLE	
						VB313AA	
						DRAW. No.	
						C1CP302570-X2	CAST
Rev.	Date	Design	Check	Appr.	Description		Sheet
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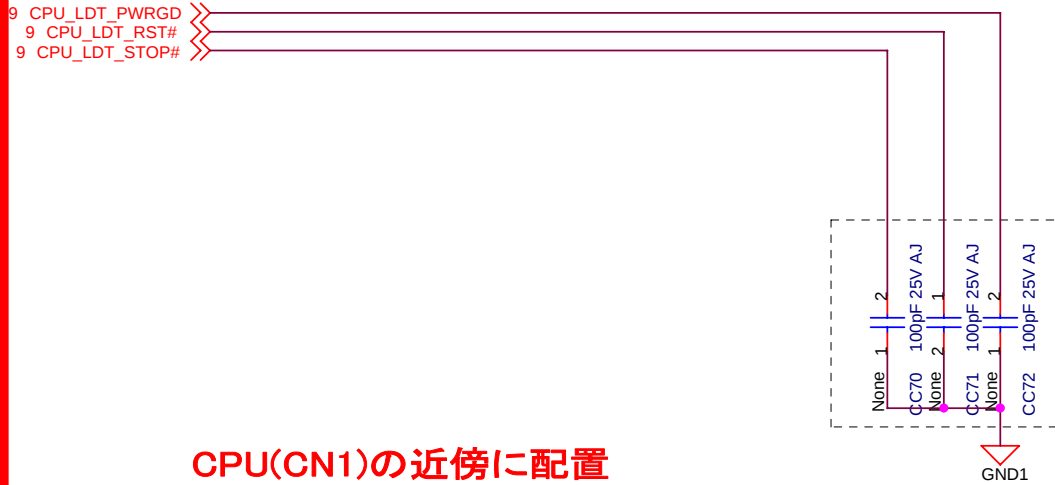
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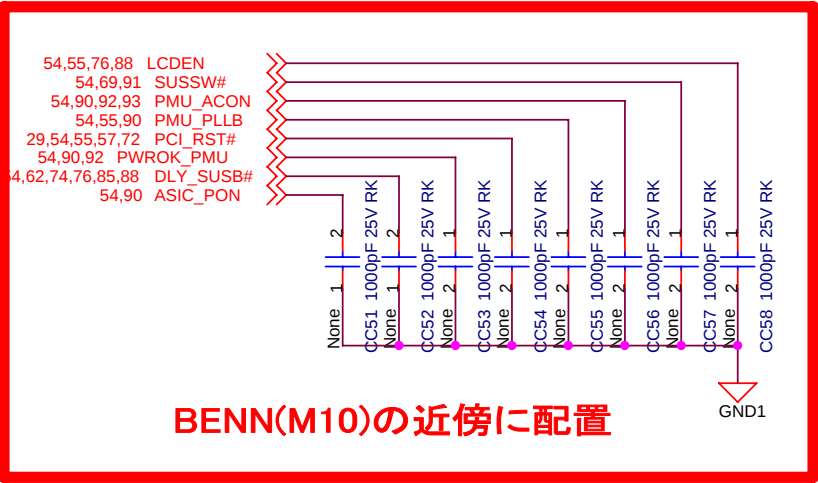
R-C for EMI

						TITLE VB313AA		
						DRAW. No.		CAST
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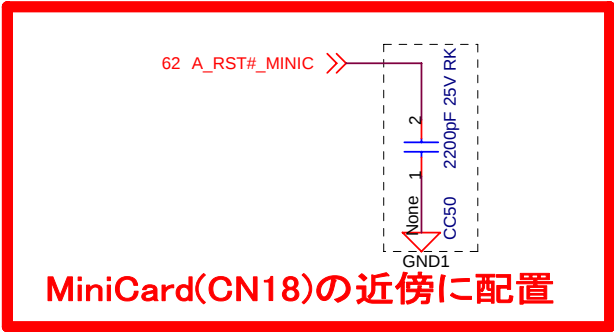
CPU(CN1)の近傍に配置



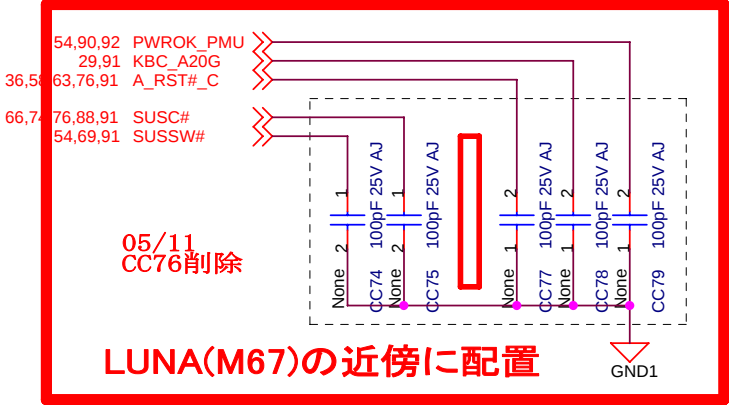
BENN(M10)の近傍に配置



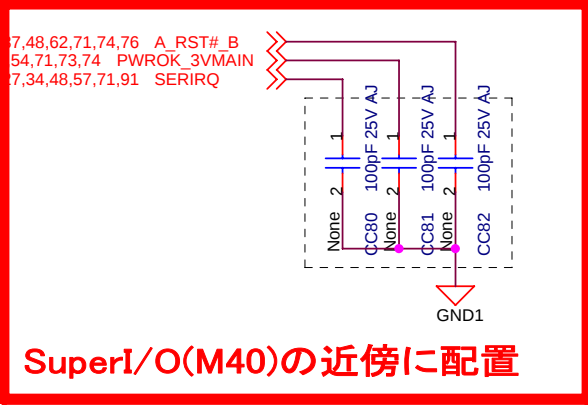
MiniCard(CN18)の近傍に配置



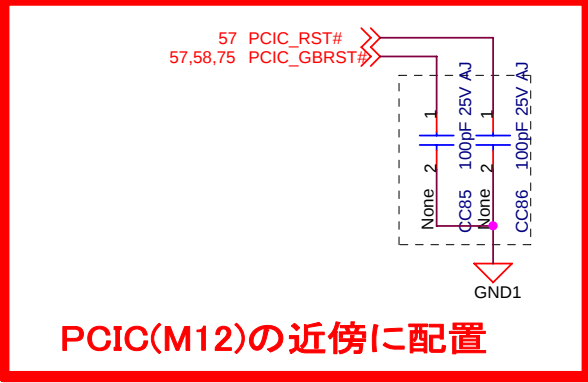
LUNA(M67)の近傍に配置



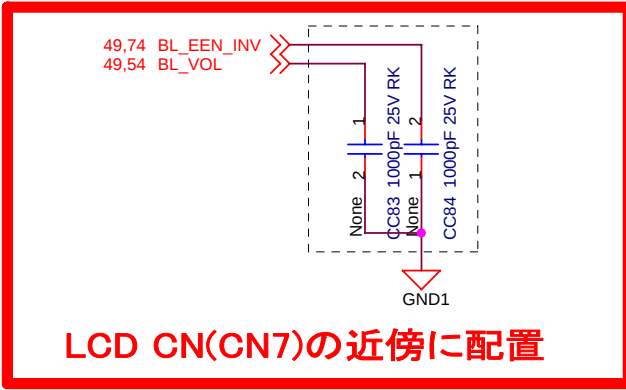
SuperI/O(M40)の近傍に配置



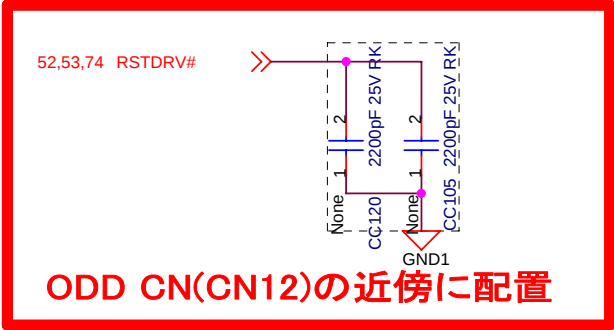
PCIC(M12)の近傍に配置



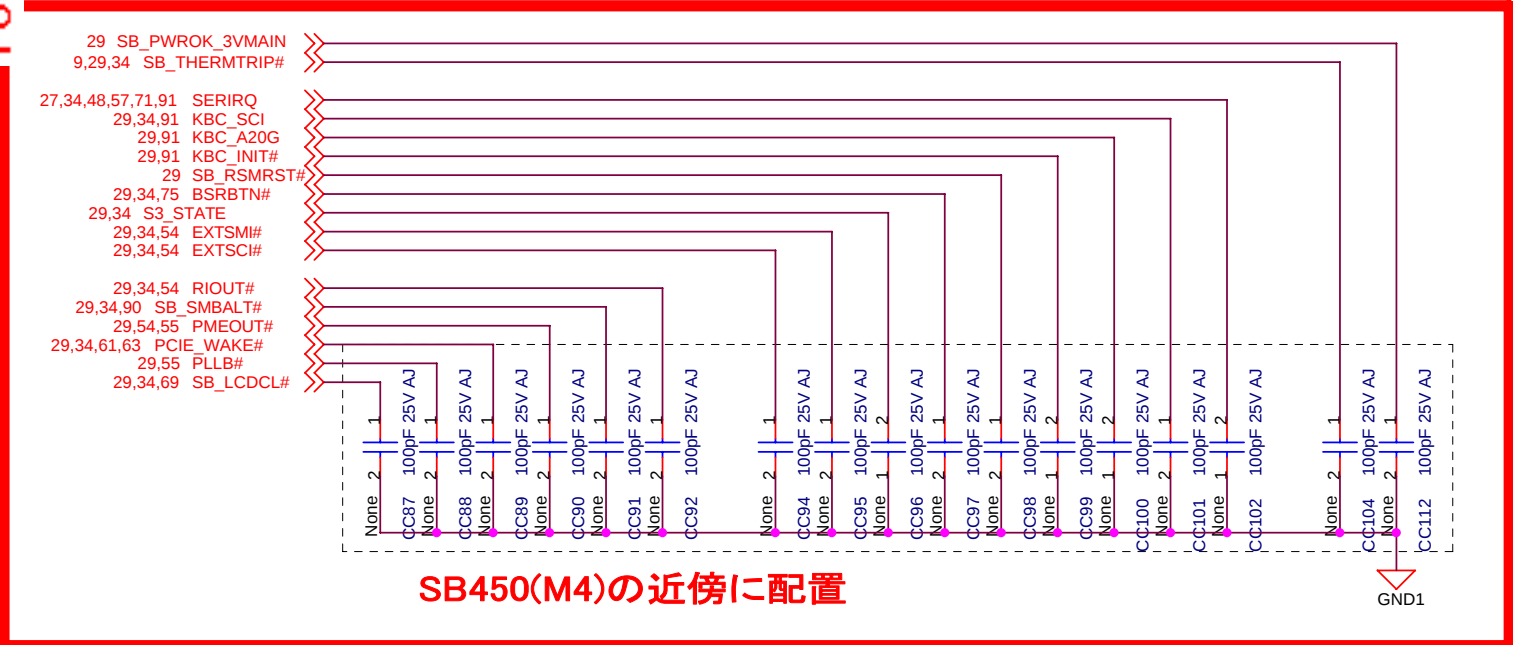
LCD CN(CN7)の近傍に配置



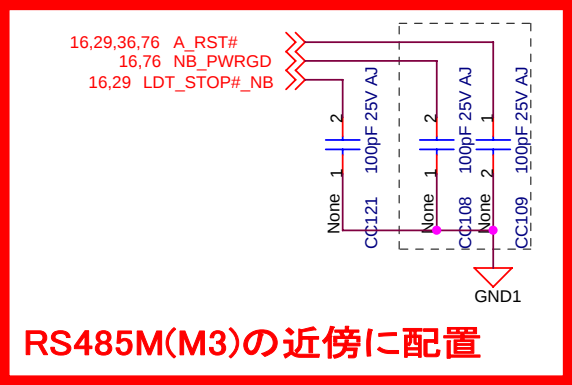
ODD CN(CN12)の近傍に配置



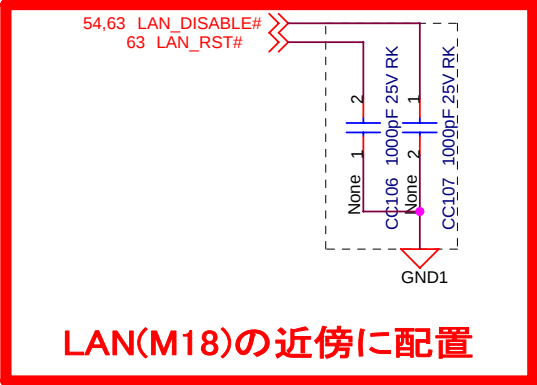
SB450(M4)の近傍に配置



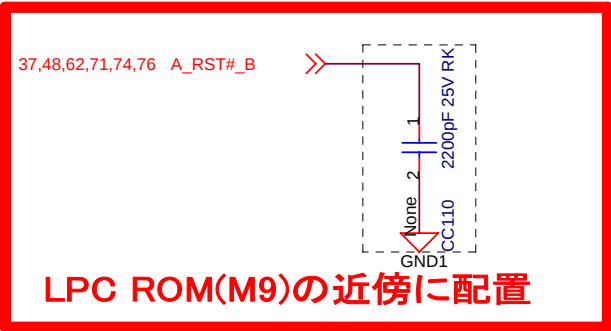
RS485M(M3)の近傍に配置



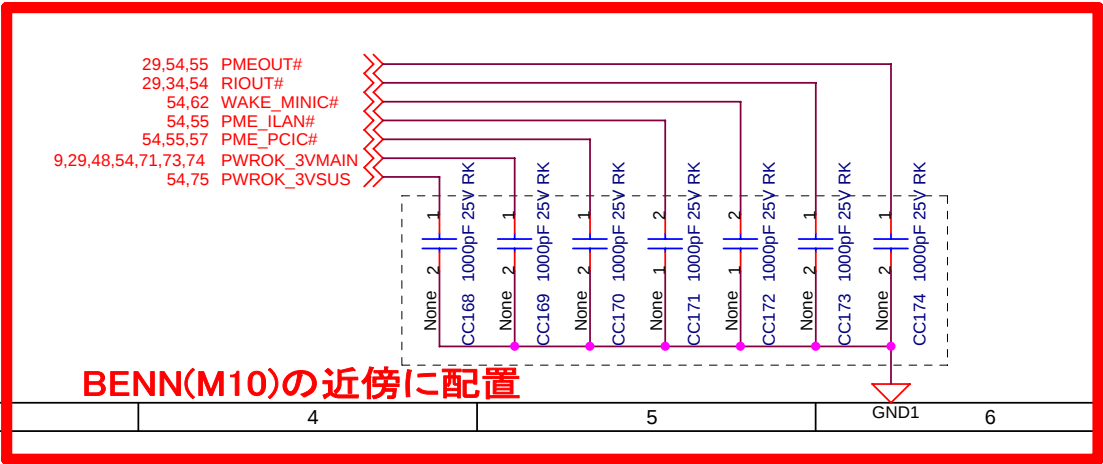
LAN(M18)の近傍に配置



LPC ROM(M9)の近傍に配置



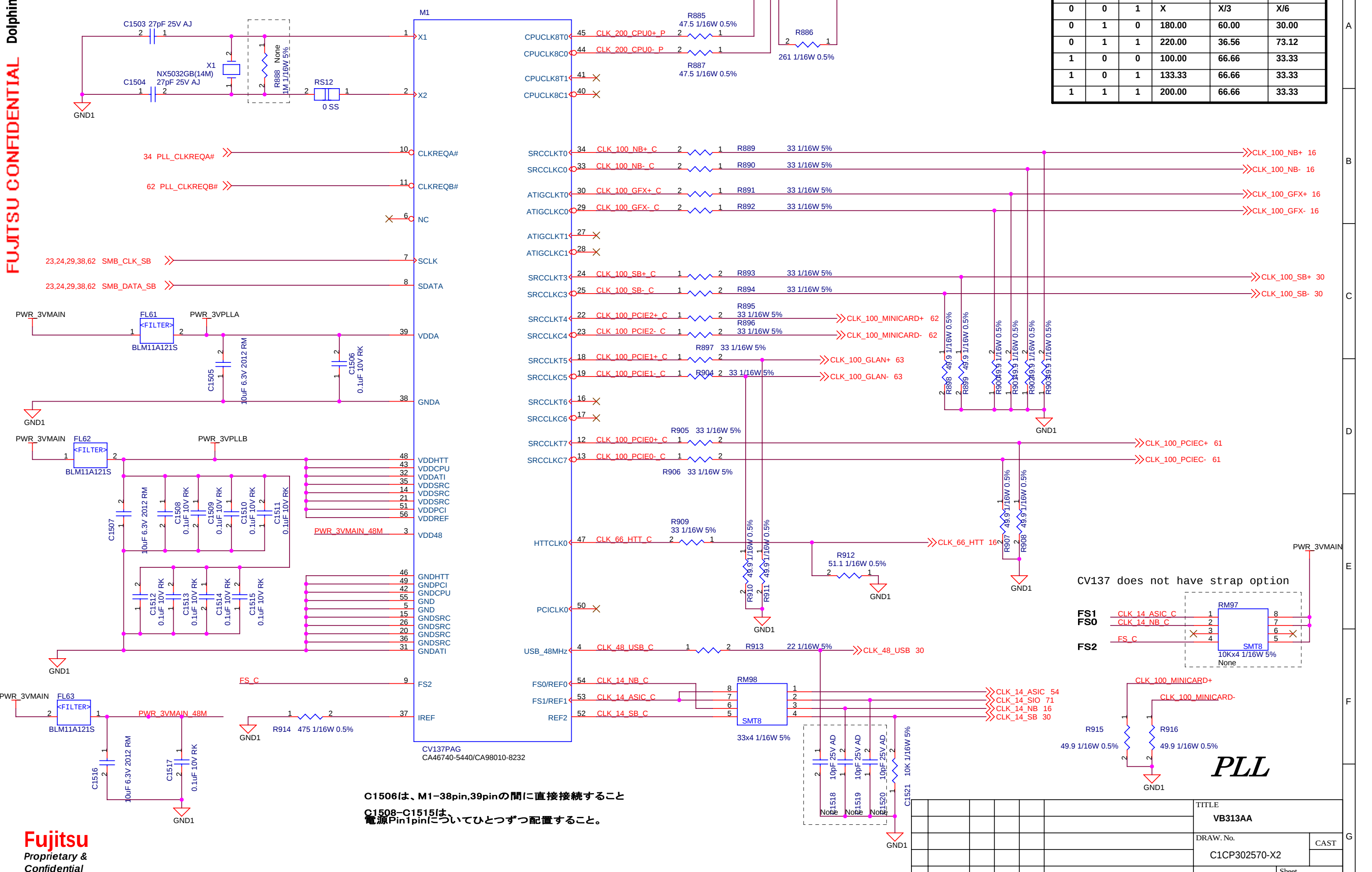
BENN(M10)の近傍に配置



R-C for ESD

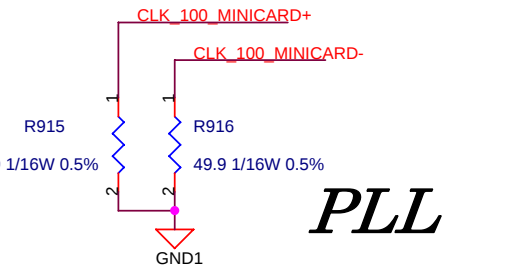
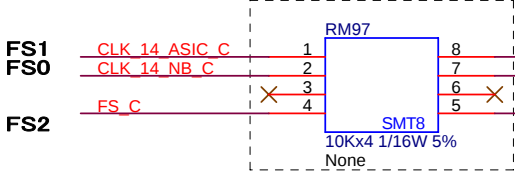
						TITLE		
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						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
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						Sheet	4 / 93	
						Appr.	Hasegawa	

X1の部品・配線の周辺・上下層はGNDでガードすること。
また、配線は極力短く行い、振動子及び周辺部品の
パッドの下層は配線禁止とする。



FS2	FS1	FS0	CPU(MHz)	HTT(MHz)	PCI(MHz)
0	0	0	Hi-Z	Hi-Z	Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	36.56	73.12
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	1	200.00	66.66	33.33

CV137 does not have strap option

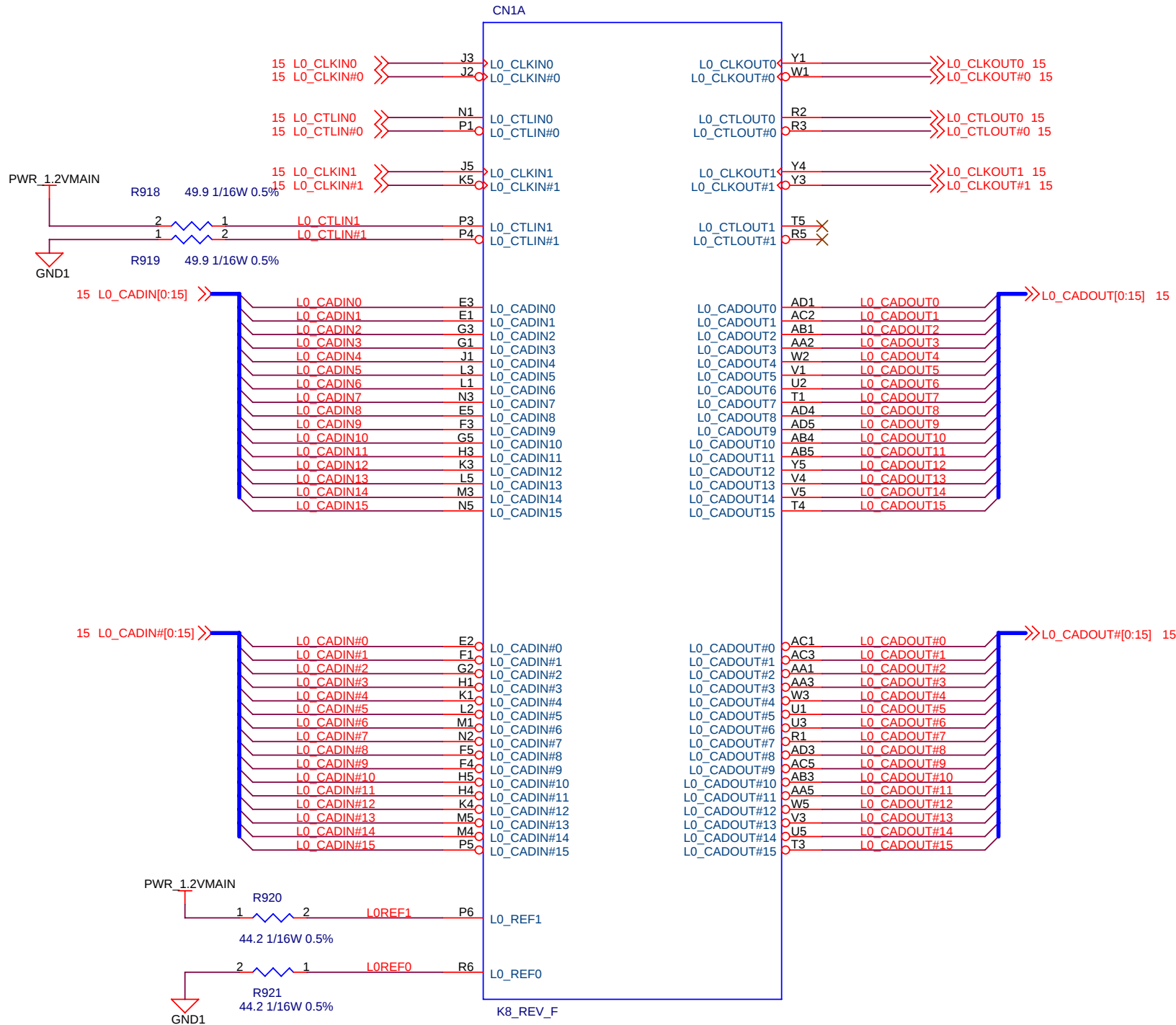
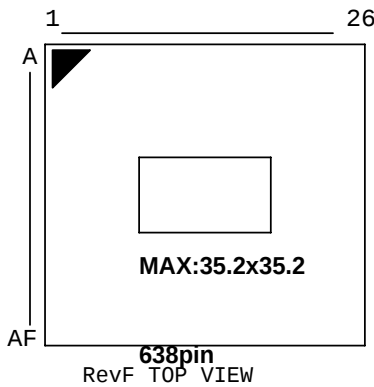


PLL

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C1506は、M1-38pin,39pinの間に直接接続すること
C1508-C1515は、
電源Pin1pinについてひとつずつ配置すること。

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						C1CP302570-X2			
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L0REF0,L0REF1は0.127mmの線幅にて配線し、
他の信号から0.254mm以上離すこと。
R920,R921は25.4mm以内に配置すること。

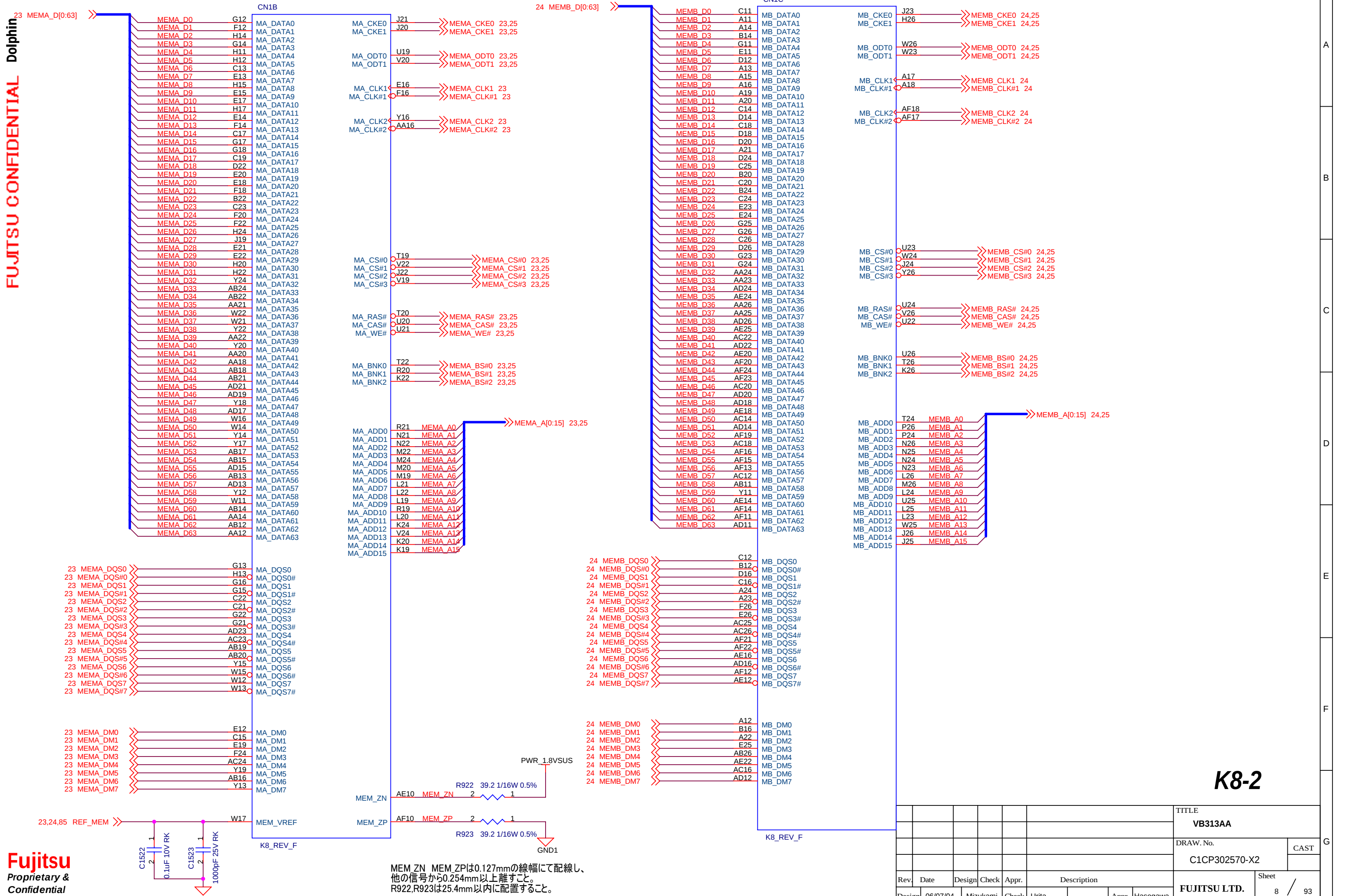
K8-1

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet 7 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

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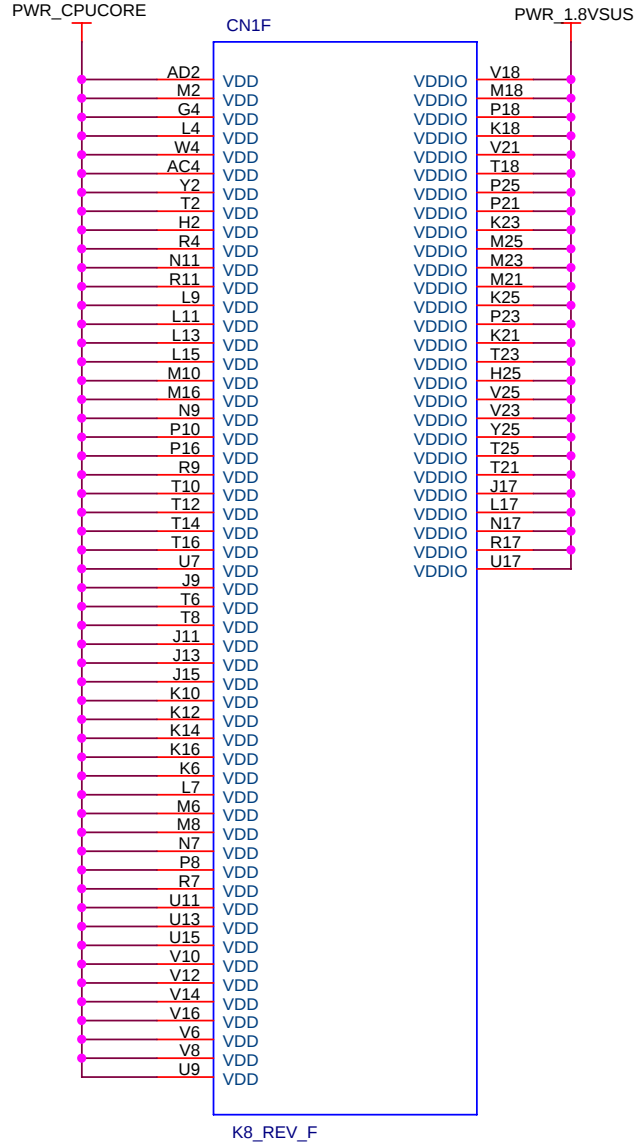
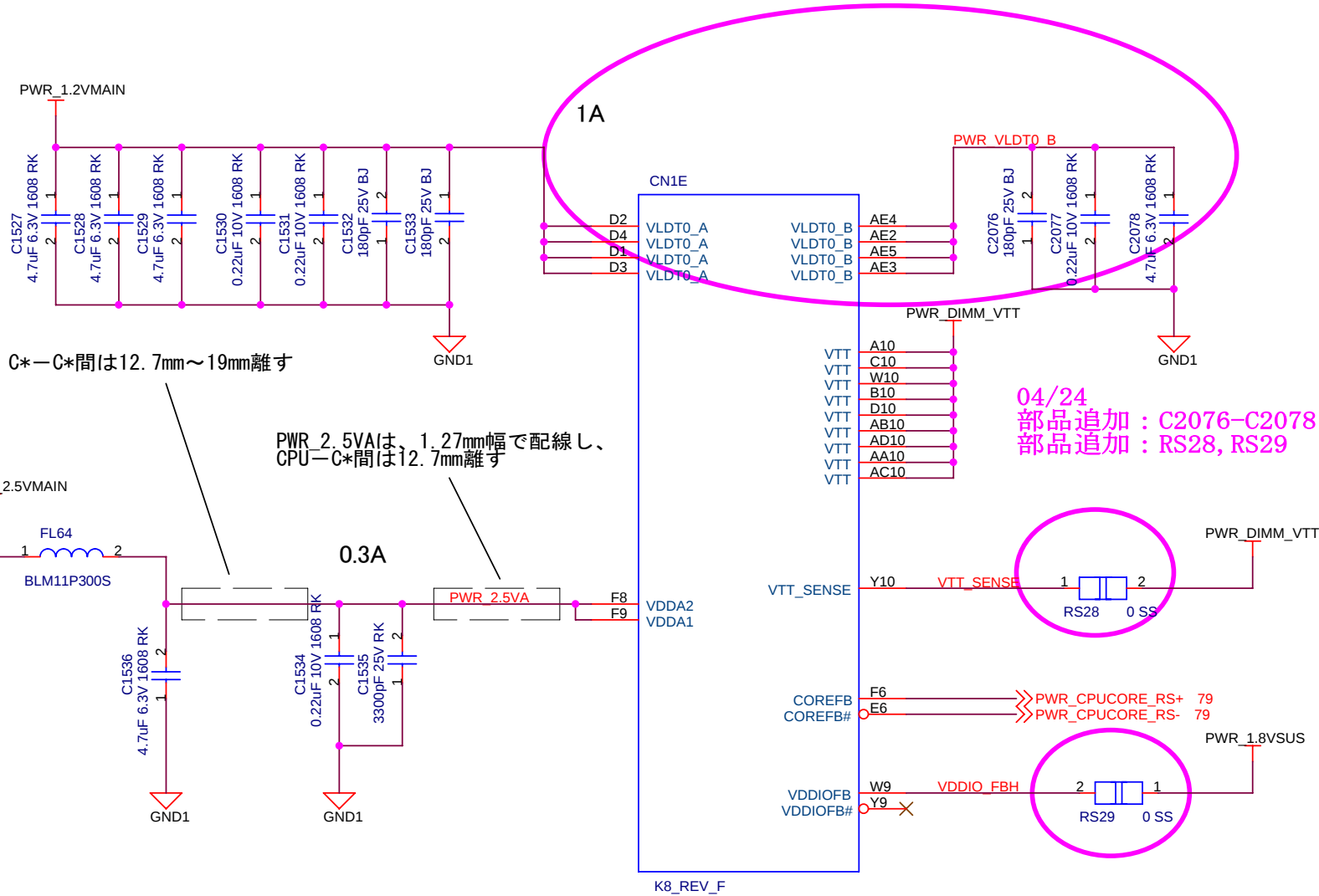
Dolphin

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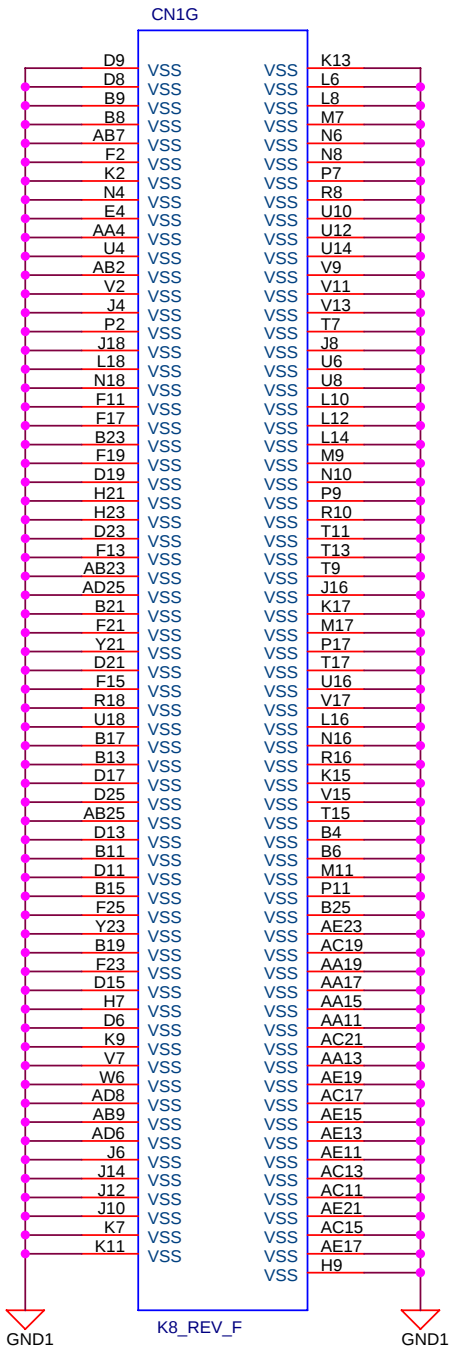
MEM_ZN, MEM_ZPは0.127mmの線幅にて配線し、
他の信号から0.254mm以上離すこと。
R922,R923は25.4mm以内に配置すること。

K8-2



						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD.
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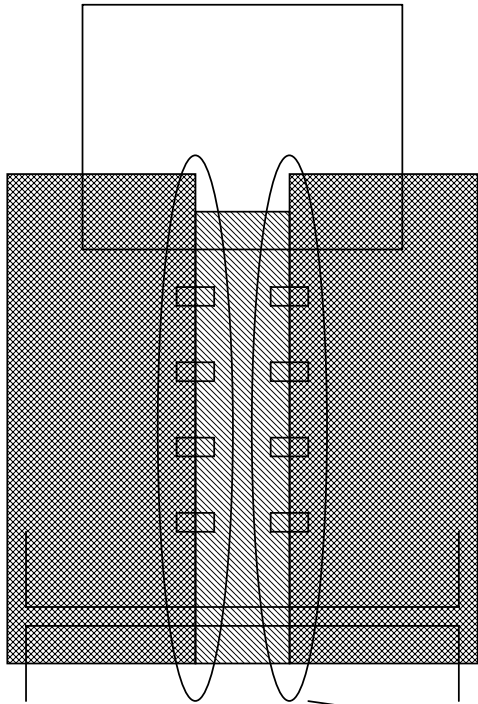
FUJITSU CONFIDENTIAL Dolphin



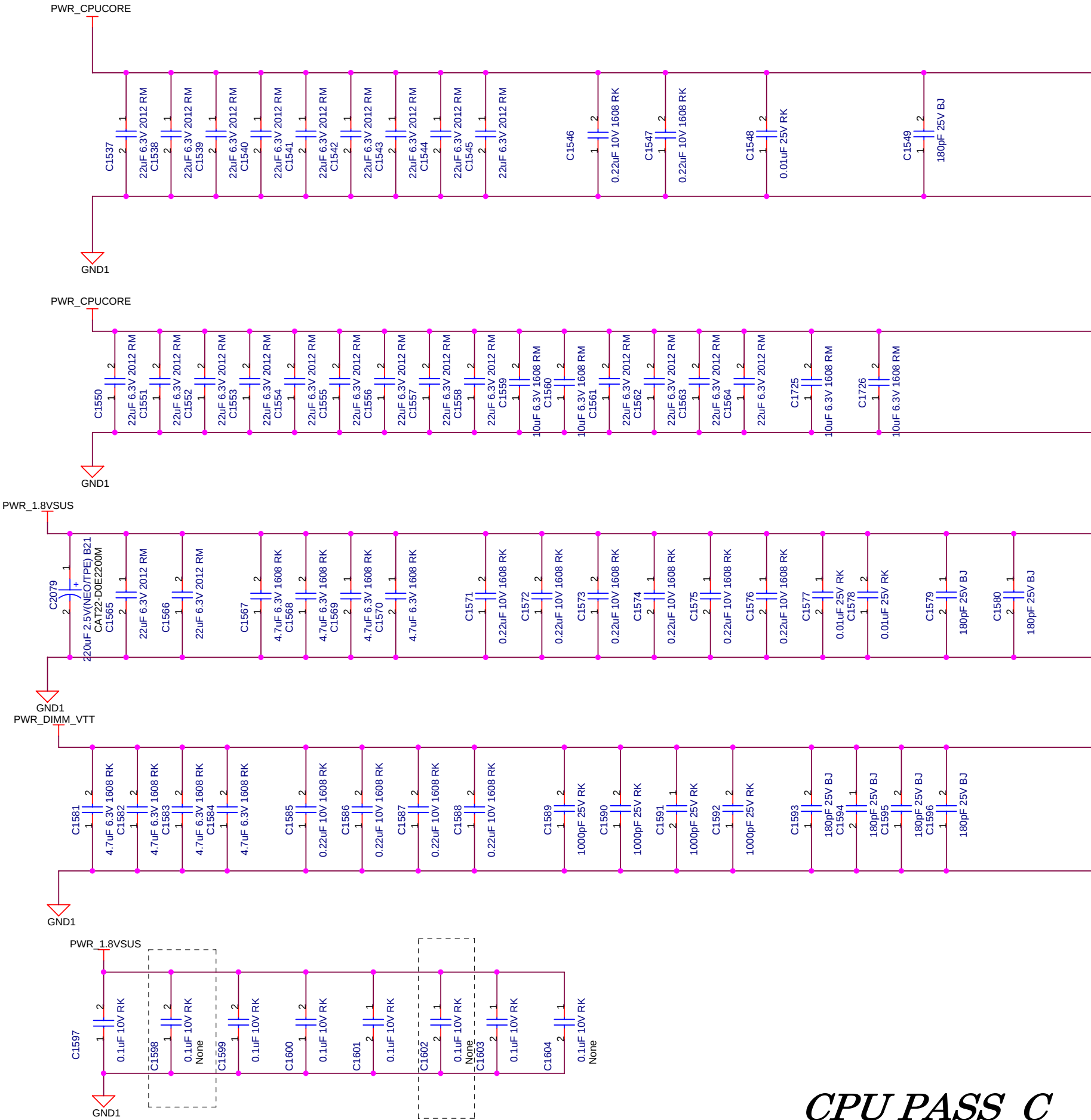
K8-5

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					DRAW. No.			CAST
					C1CP302570-X2			
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これらのコンデンサC1597～C1604は、図のように
PWR_1.8VSUS, GND1のプレーンの間に
約1インチ間隔で配置すること。

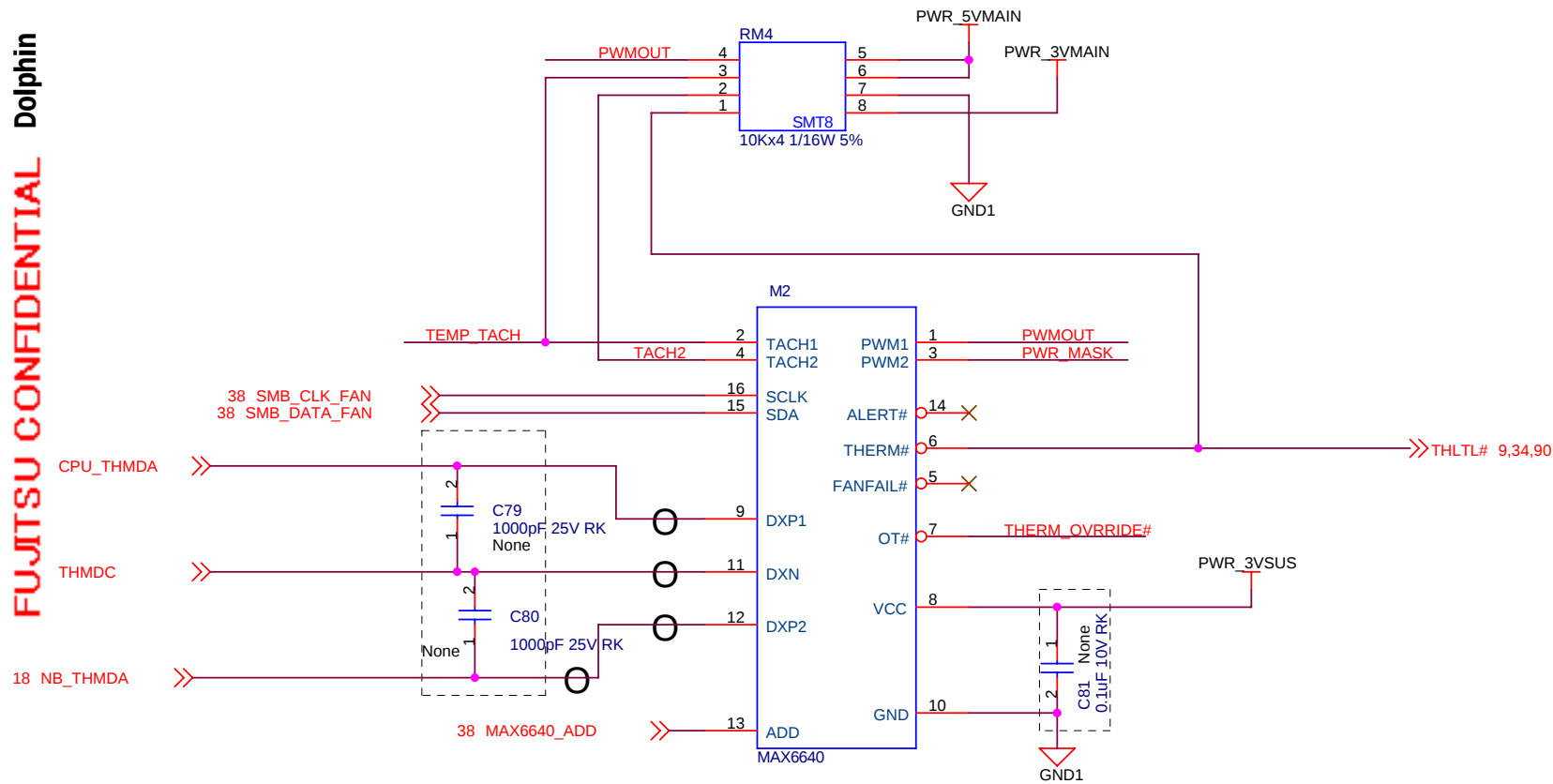


K8_CPU

CPU PASS_C

						TITLE		
						VB313AA		
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B																B	
C																C	
D																D	
E																E	
F																F	
G		</															



*CPU_THMDA,
CPU_THMDCのパターンが最短に
なるよう、M2は、CPUの近傍に
配置すること。*

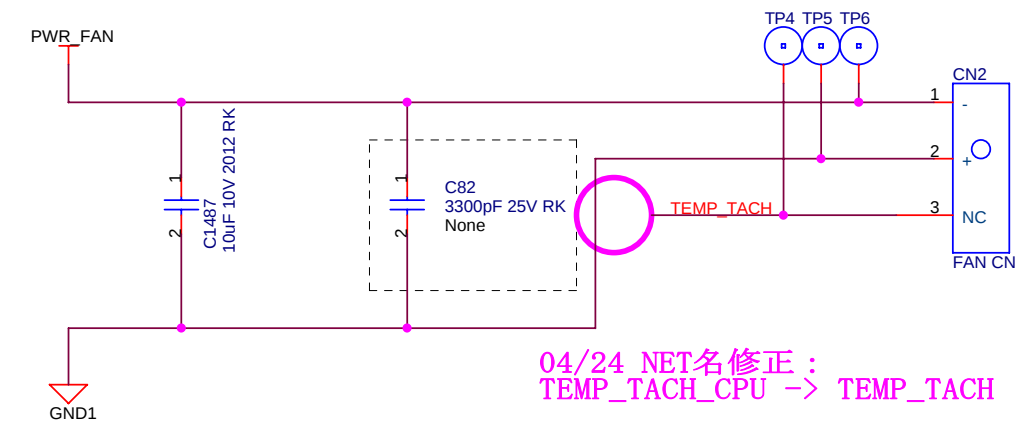
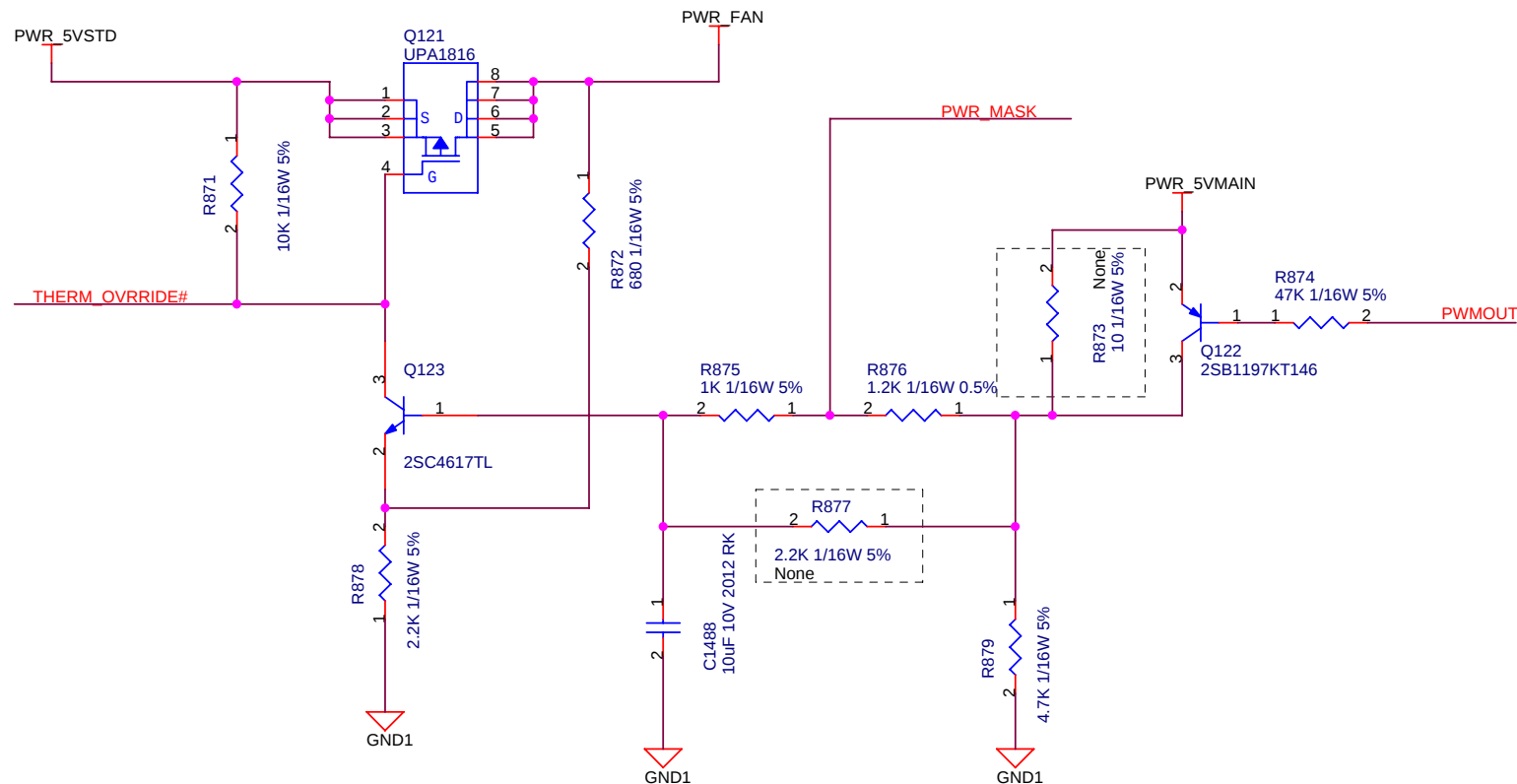
CPU THMDA, CPU THMDC, NB THMDCA 両端に入っているコンデンサ C79, C80 (1000pF) は、M2 の直近に配置すること。

○印の付いた信号線は、GND1で両側をガードすること
(下図参照)

10mil (	
10mil (	
10mil (	
10mil (	

MAX6640
SMBAddress:01011110[5E固定]

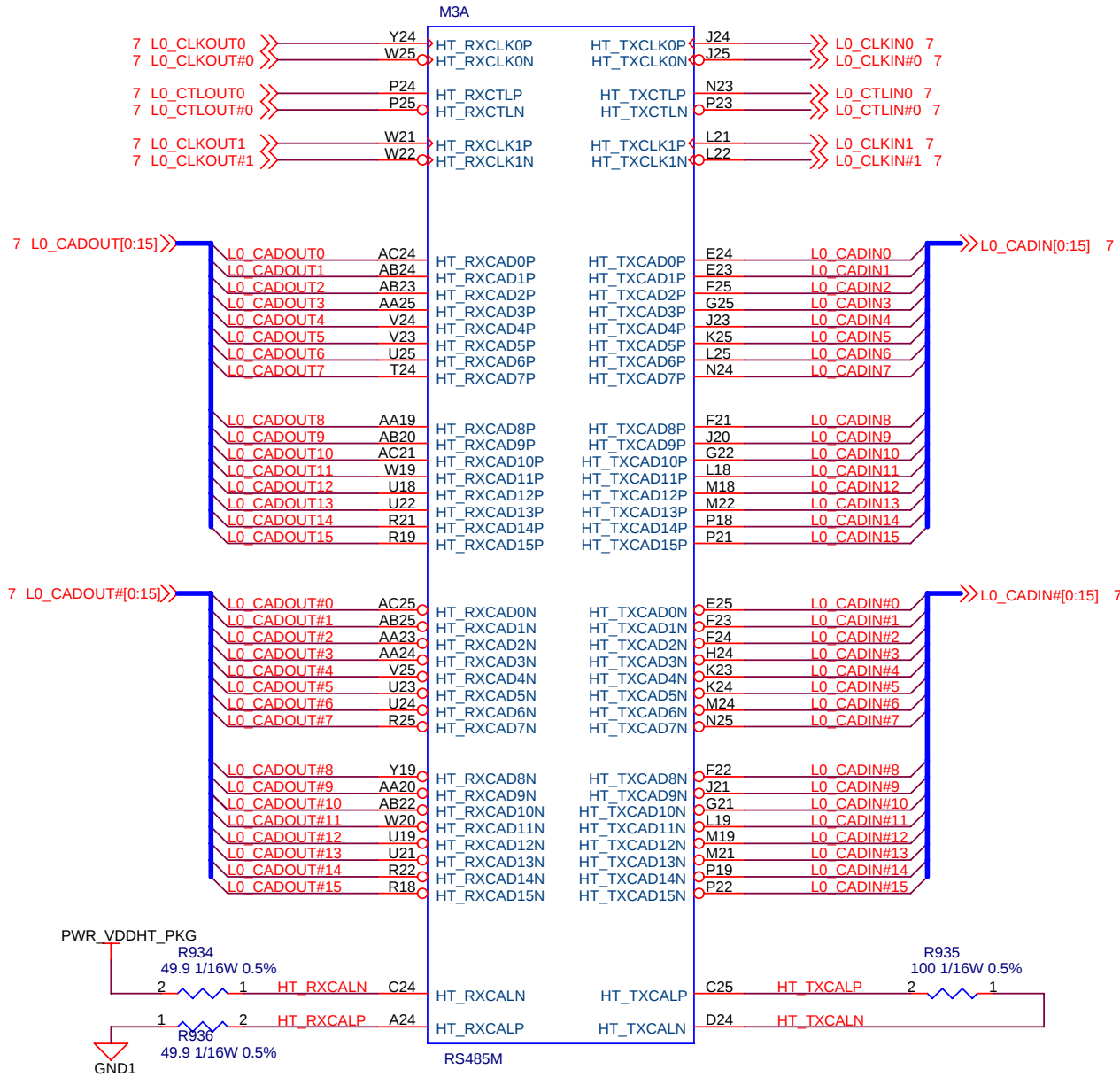
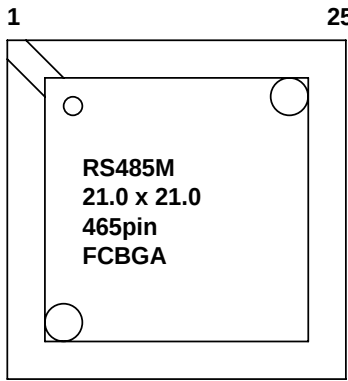
5.0V 0.3A



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以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
PLLVSS (B10pin)

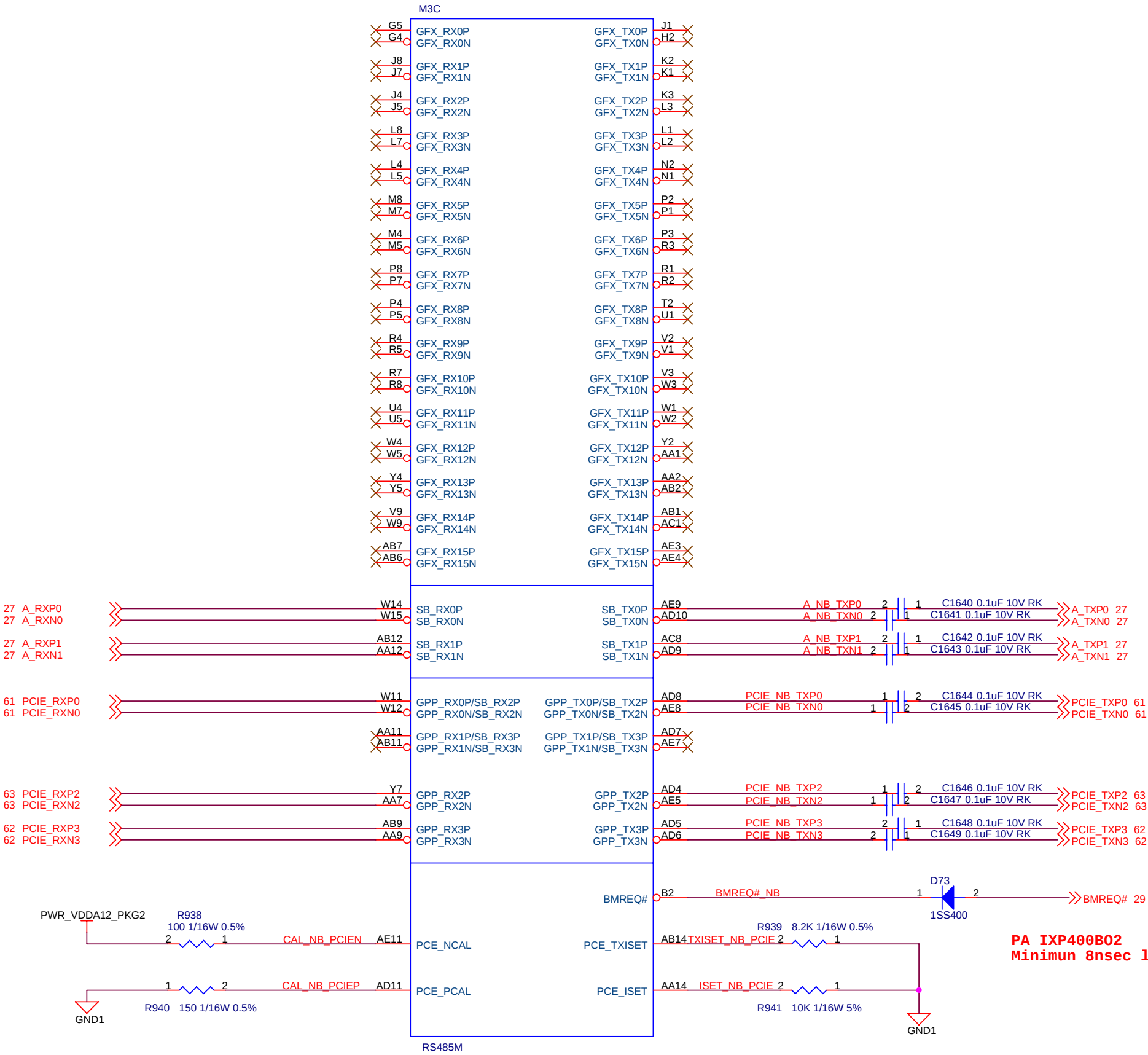
以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1607 : PLLVDD (A10pin) とPLLVSS (B10pin) の間

FOR RS690 ONLY

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1606 : HTPVDD (B24pin) とHTPVSS (B25pin) の間

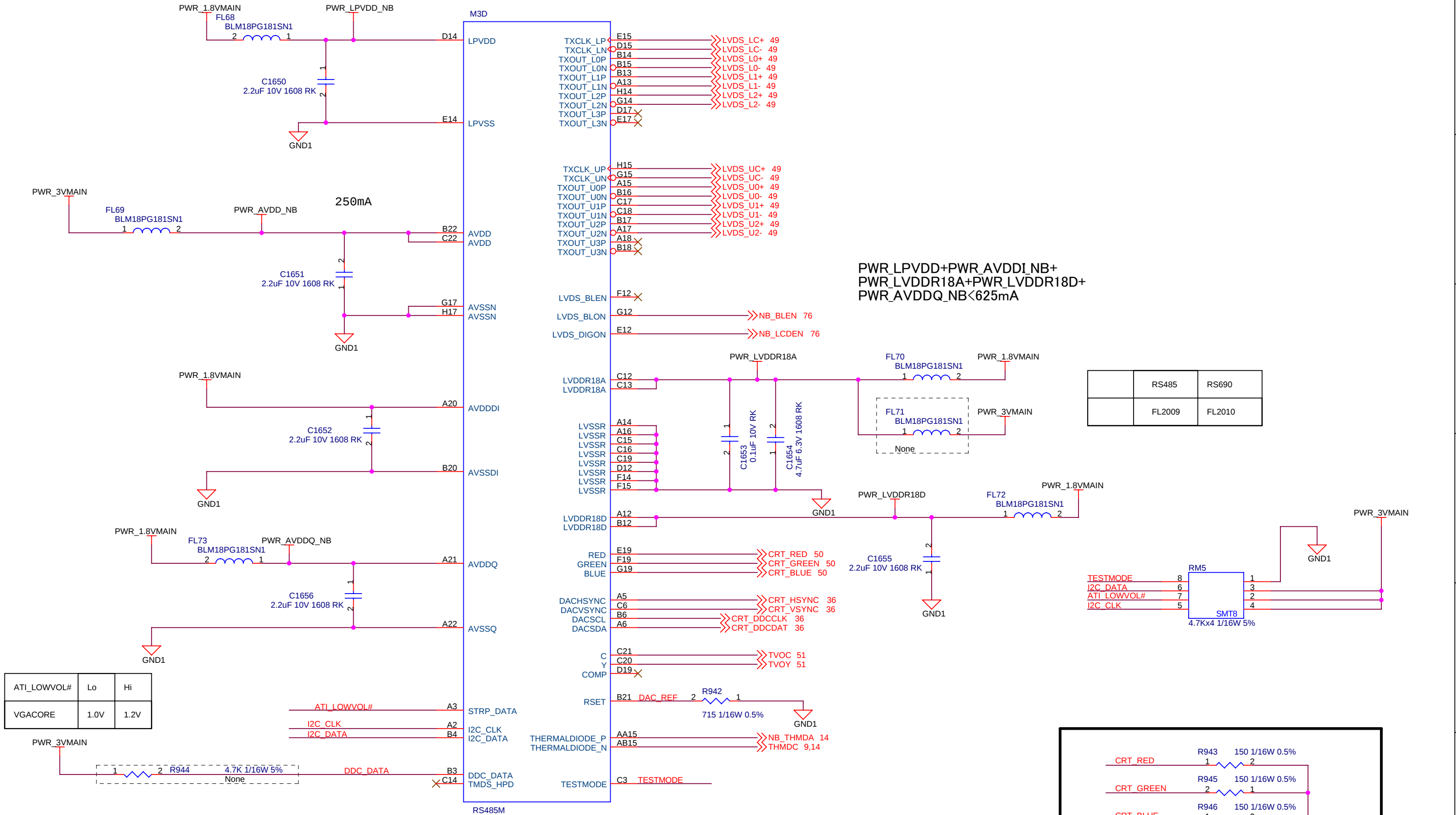
RS485-2

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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
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						TITLE		
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
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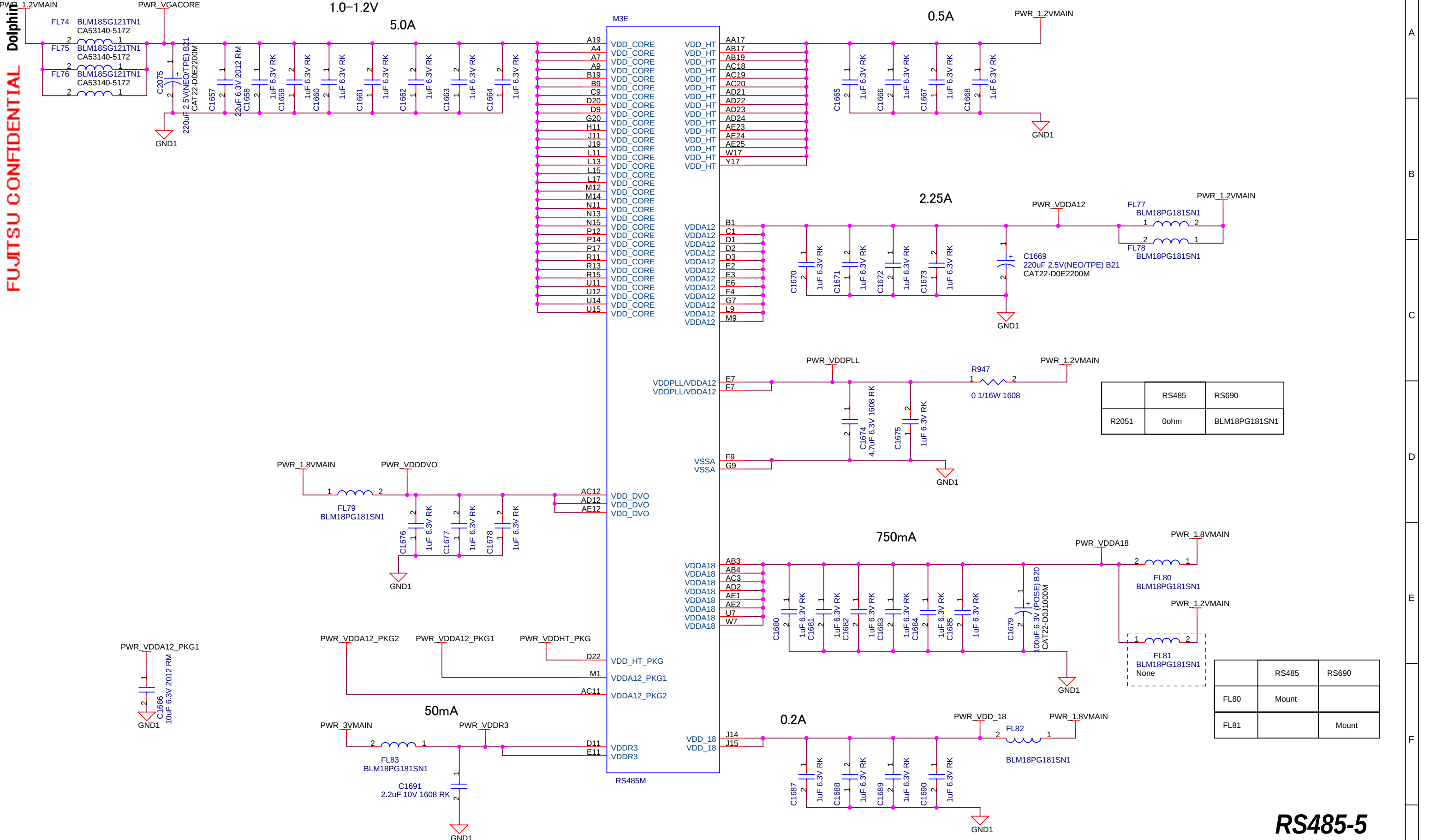
以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
LPVDD(D14pin)とLPVSS(E14pin)の間
LPVSS(E14pin)
LVSSR(A14,A16,C15,C16,C19,D12,F14,F15pin)の間
AVSSN(G17,H17pin)の間
AVSSDI(B20pin)の間
AVSSQ(A22pin)の間

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1650 : LPVDD(D14pin)とLPVSS(E14pin)の間
C1653, C1654 : LVDDR18A(C12,C13pin)とLVSSR(A14,A16,C15,C16,C19,D12,F14,F15pin)の間
C1651 : AVDD(B22,C22pin)とAVSSN(G17,H17pin)の間
C1652 : AVDDI(A20pin)とAVSSDI(B20pin)の間
C1656 : AVDDQ(A21pin)とAVSSQ(A22pin)の間

R943,R945,R946は、M3(RS485M)の直近に配置すること

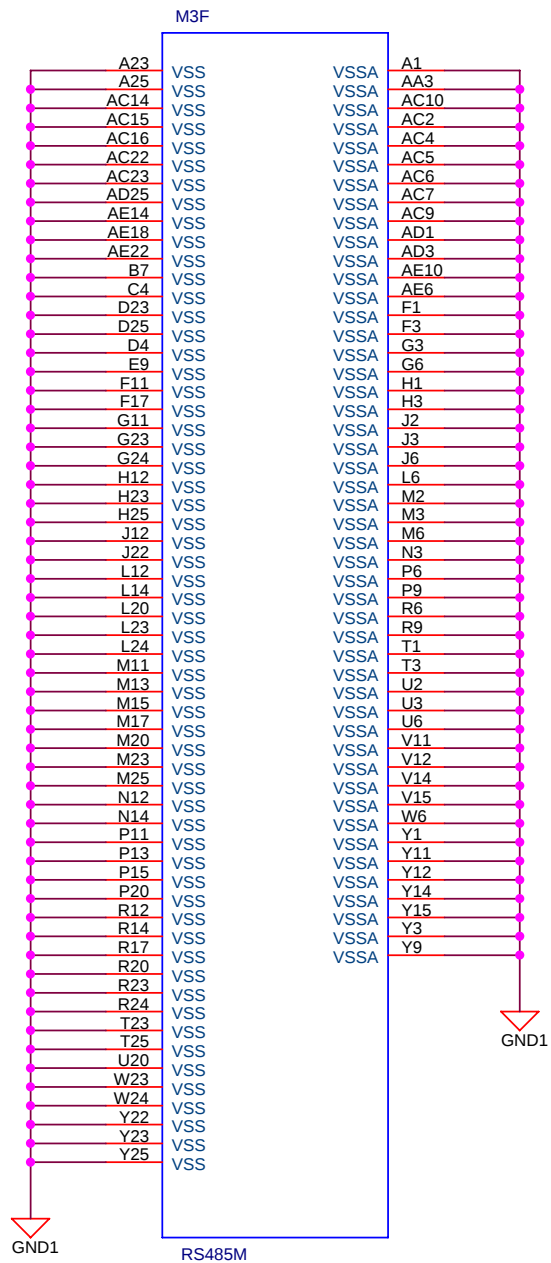
RS485-4

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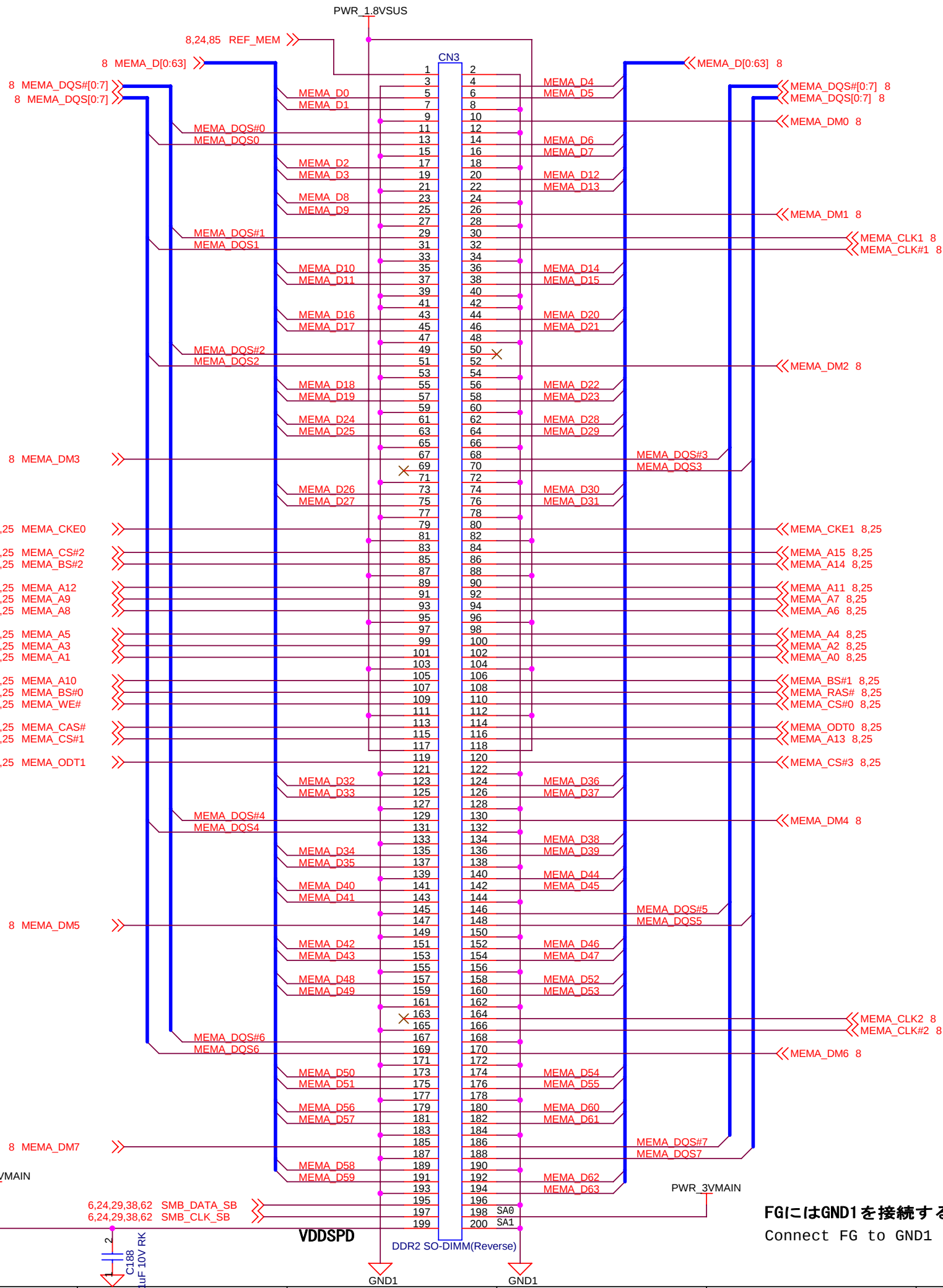


RS485-6

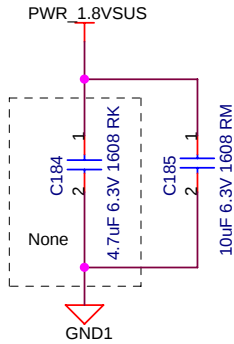
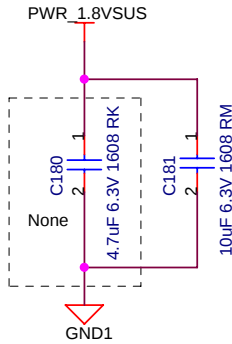
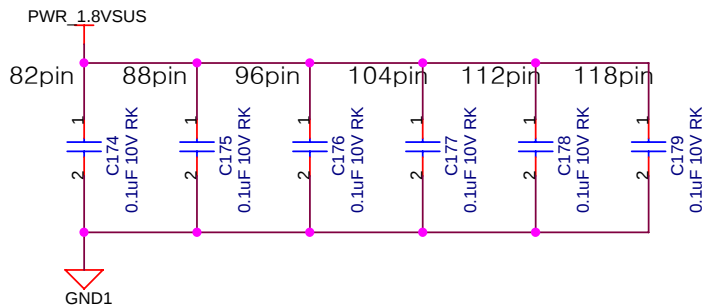
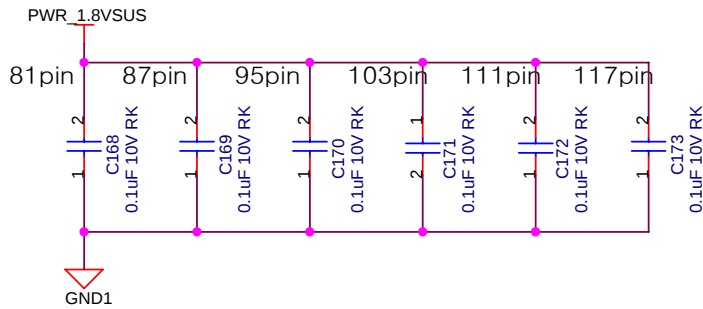
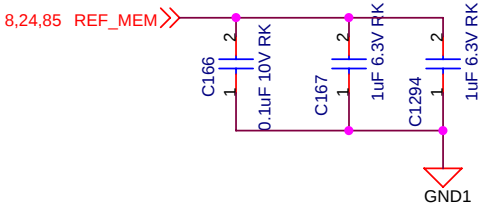
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Rev.	Date	Design	Check	Appr.	Description			Sheet
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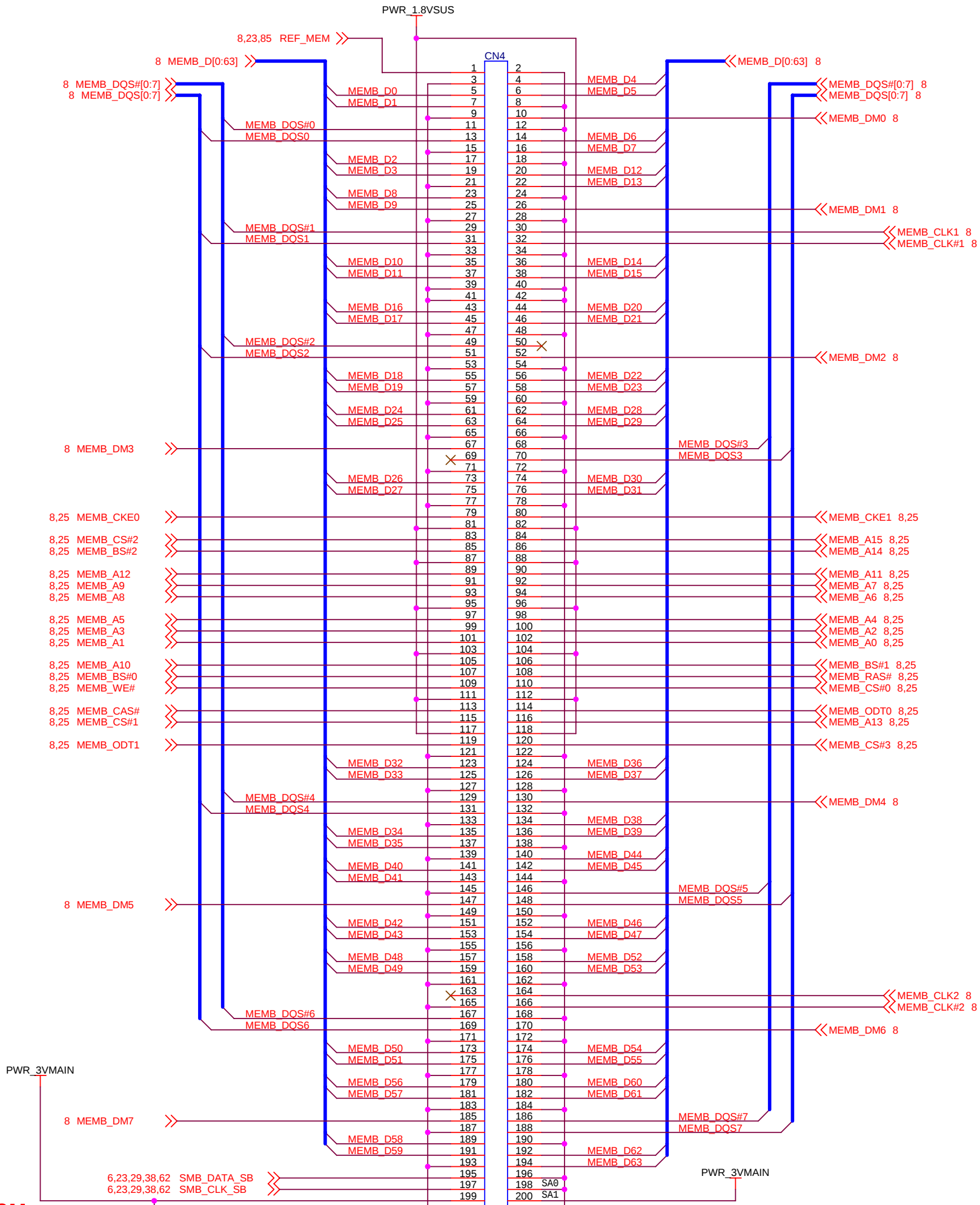


FGにはGND1を接続すること。
Connect FG to GND1



Memory Slot1

						TITLE		
						VB313AA		
						DRAW. No.		CAST
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						23 / 93		



DIMM0 SPD address : A4
FGにはGND1を接続すること。
Connect FG to GND1

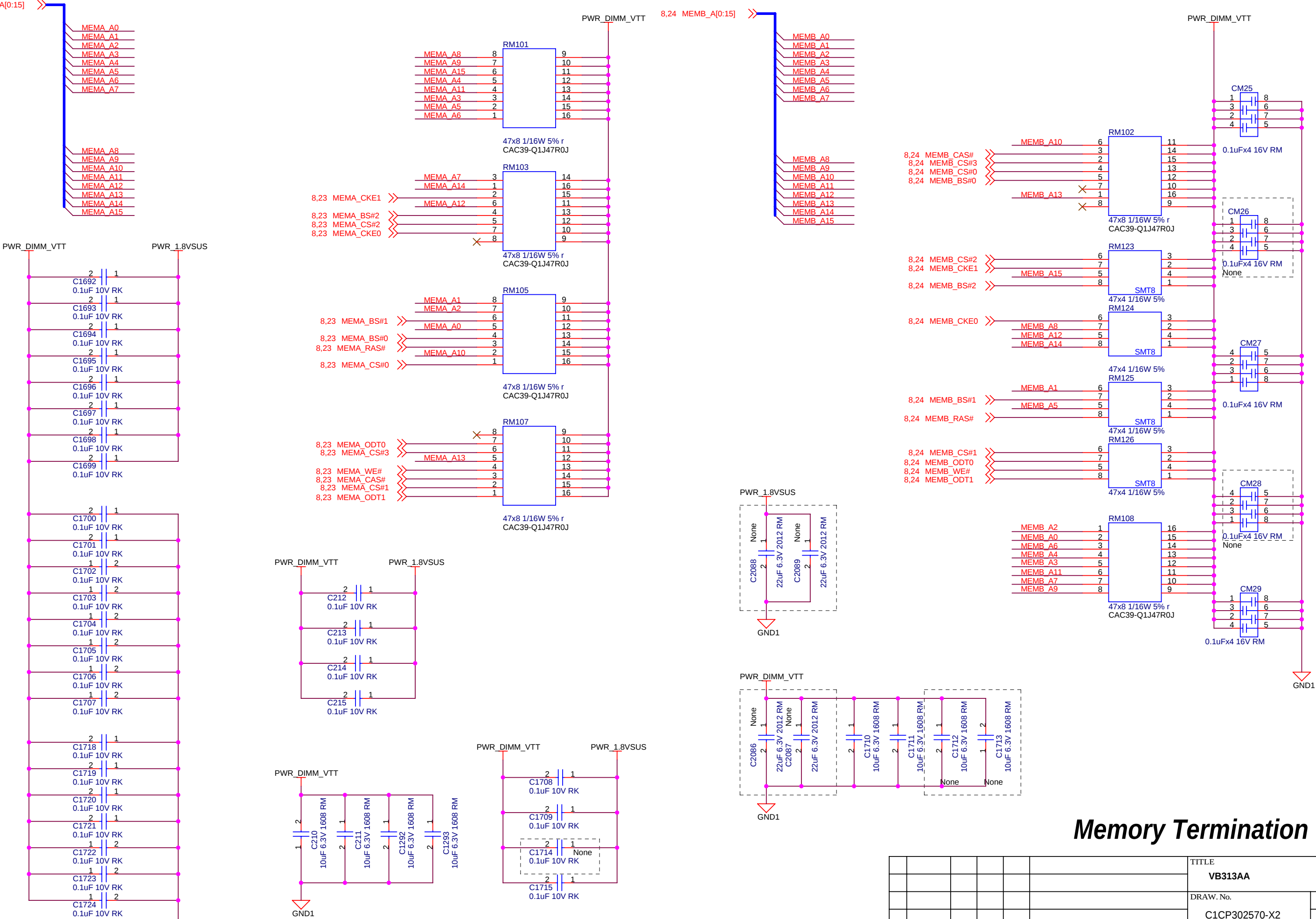
Memory Slot2

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						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
Design	06/07/04	Mizukami	Check	Urita				
						Sheet		
						24 / 93		

本ページの集合抵抗内でピンスワップ可

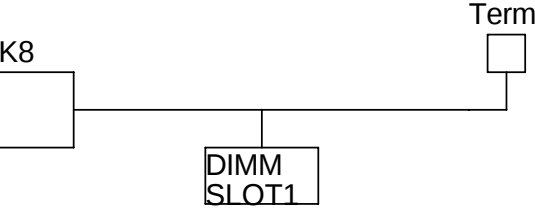
Memory Termination

						TITLE VB313AA			DRAW. No. C1CP302570-X2		CAST
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.		Sheet 25 / 93	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa				

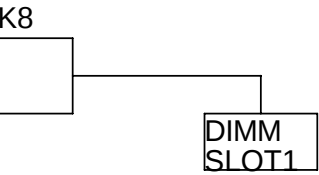


Channel A

DIMM Address/Command Topology

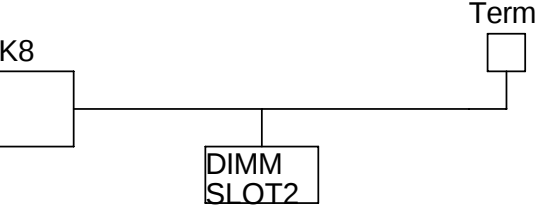


DIMM Data Bus Topology

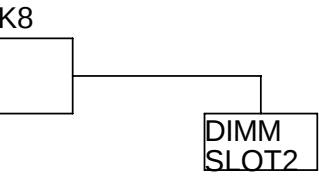


Channel B

DIMM Address/Command Topology

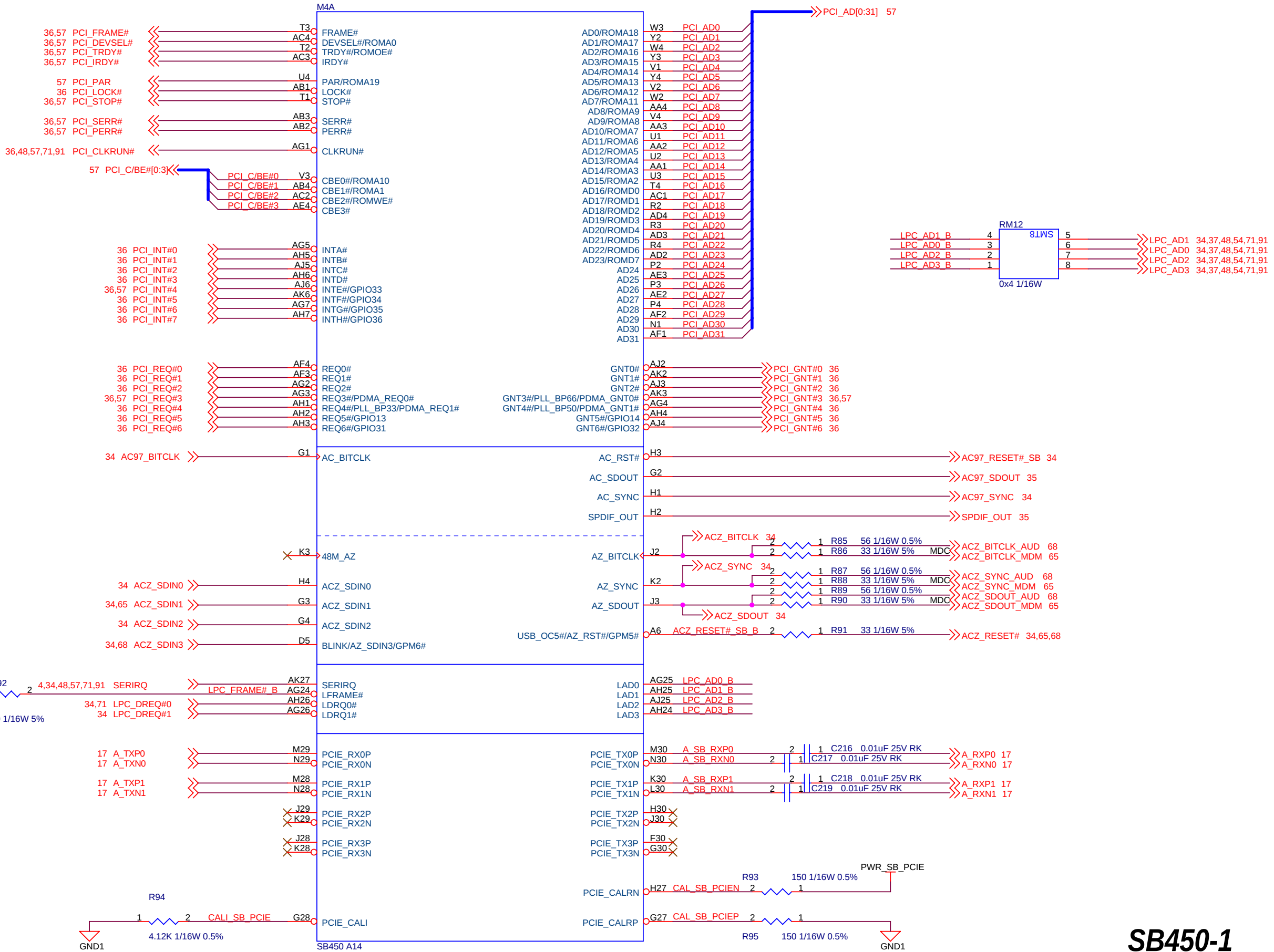
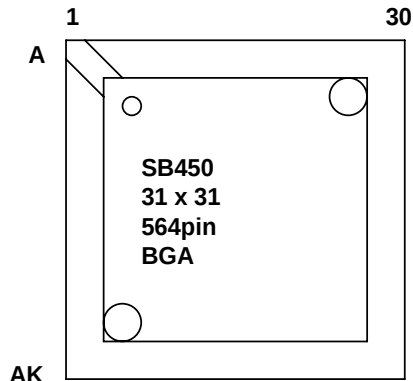


DIMM Data Bus Topology



Topology

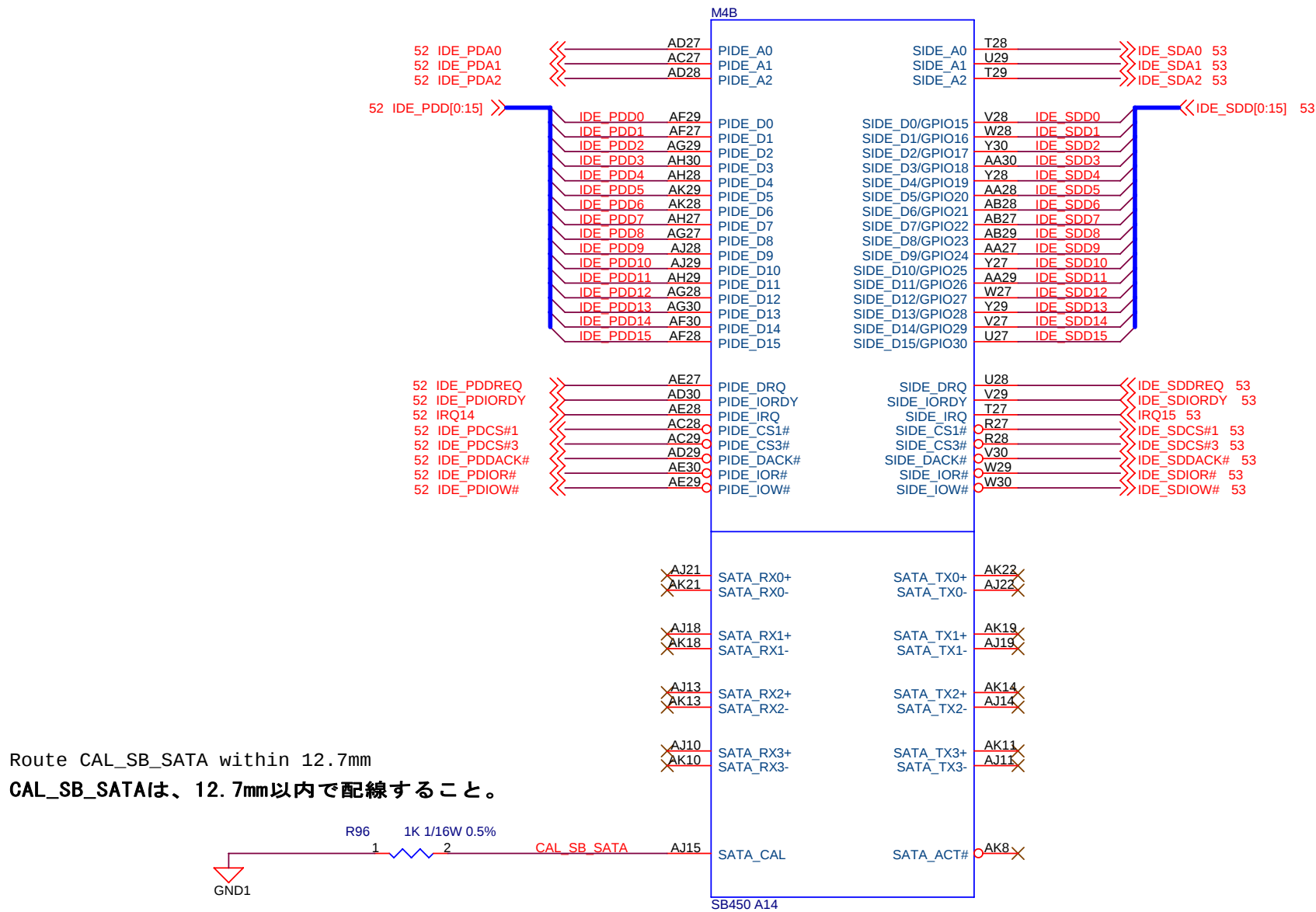
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Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 26 / 93



SB450-1

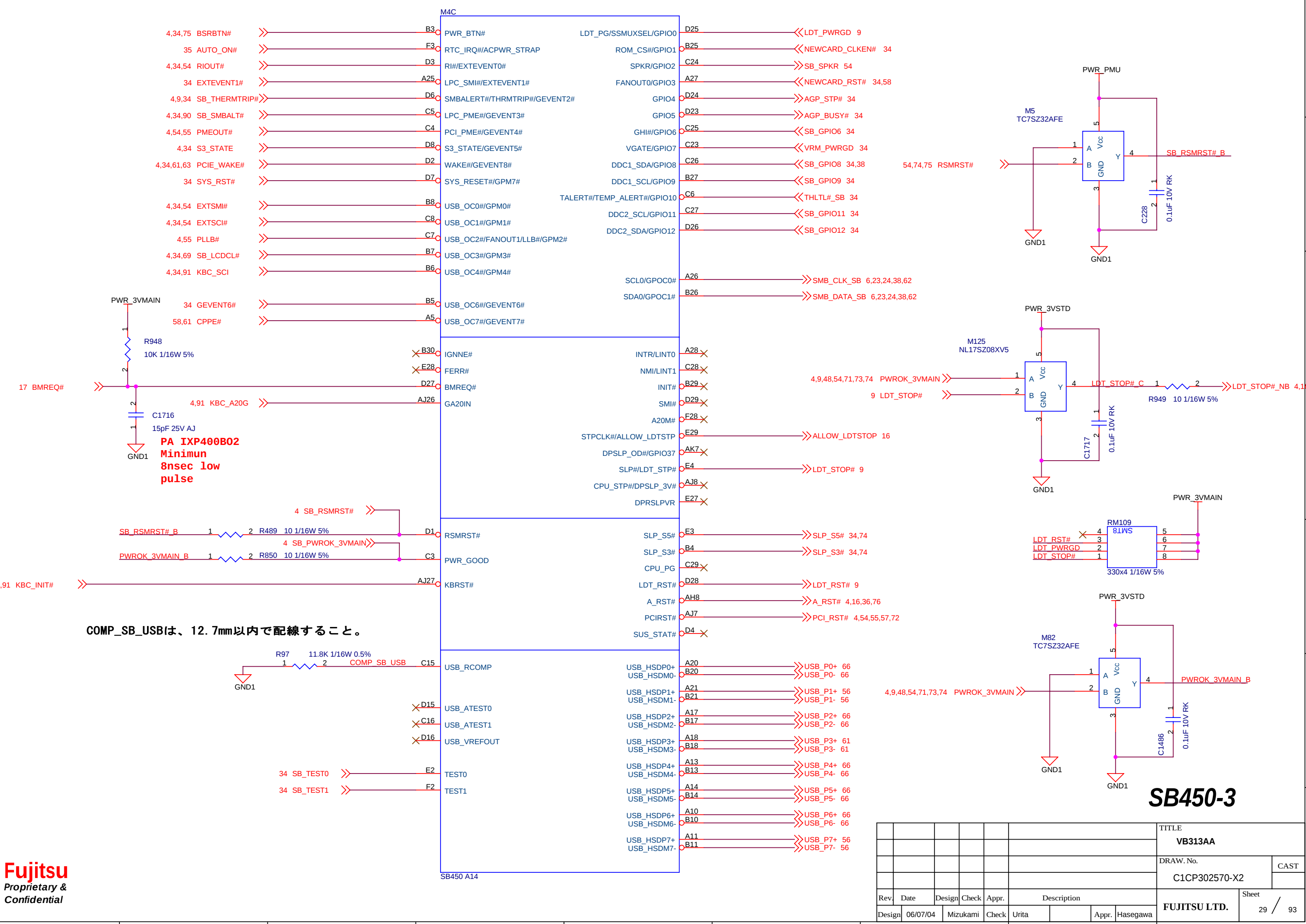
R94はG28pinから12.7mm以内に配置すること。
R93はH27pinから12.7mm以内に配置すること。
R95はG27pinから12.7mm以内に配置すること。

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		FUJITSU LTD.		27 / 93



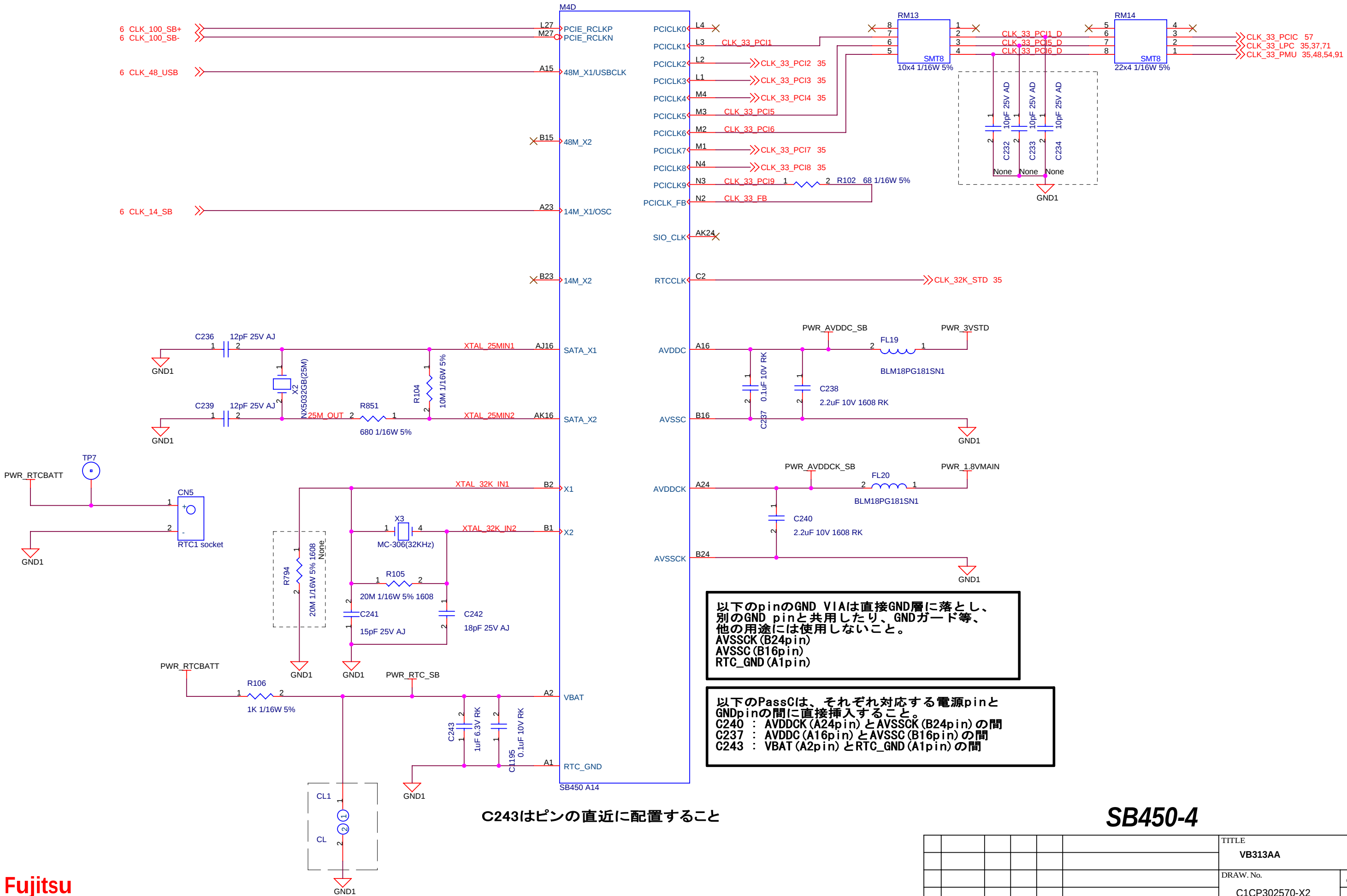
SB450-2

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Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 28 / 93



SB450-3

						TITLE		
						VB313AA		
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Design	06/07/04	Mizukami	Check	Urita				
						Sheet		
						29 / 93		

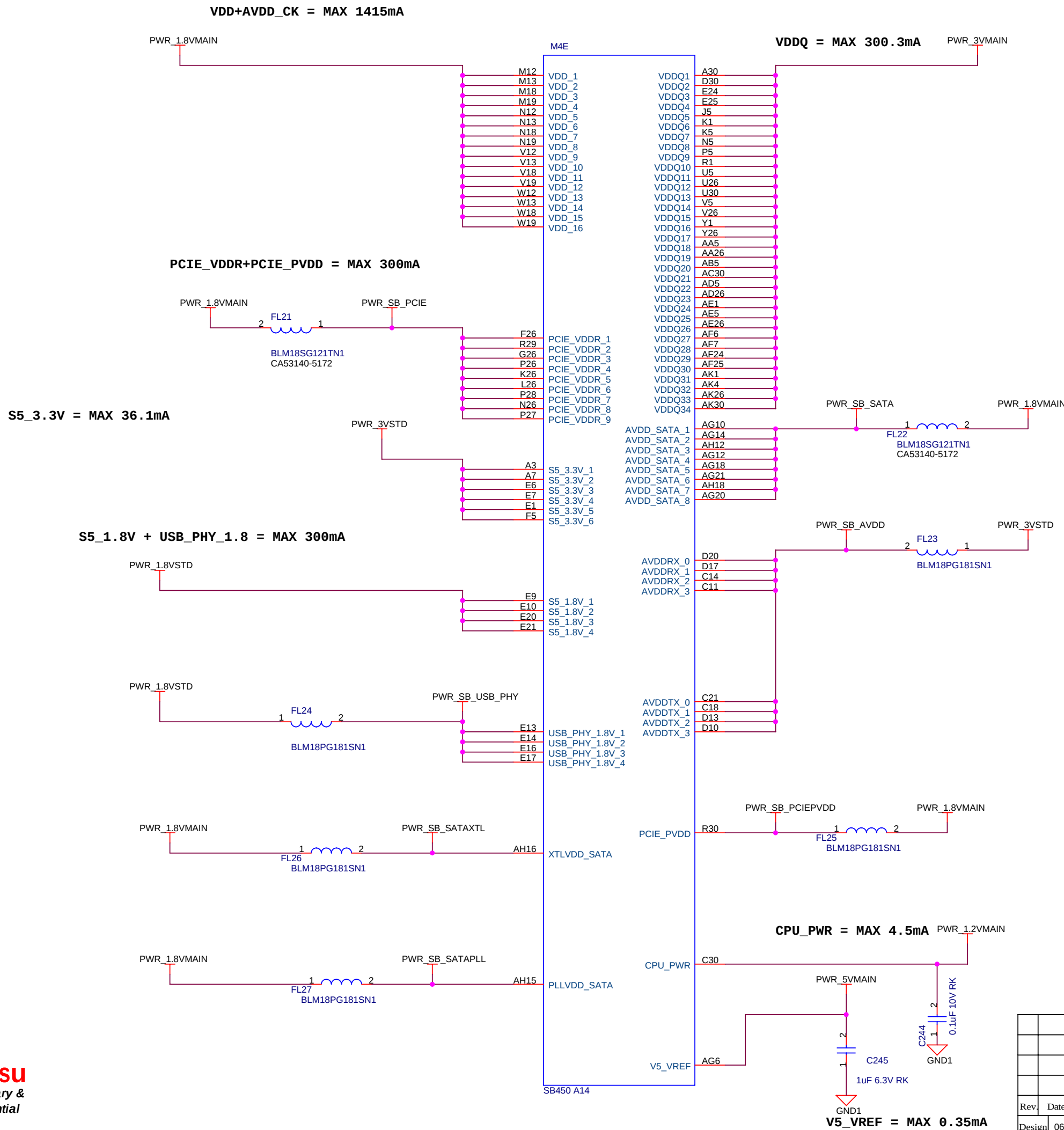


以下のpinのGND VIAは直接GND層に落とし、
別のGND pinと共用したり、GNDガード等、
他の用途には使用しないこと。
AVSSCK (B24pin)
AVSSC (B16pin)
RTC_GND (A1pin)

以下のPassCは、それぞれ対応する電源pinと
GNDpinの間に直接挿入すること。
C240 : AVDDCK (A24pin) とAVSSCK (B24pin) の間
C237 : AVDDC (A16pin) とAVSSC (B16pin) の間
C243 : VBAT (A2pin) とRTC_GND (A1pin) の間

SB450-4

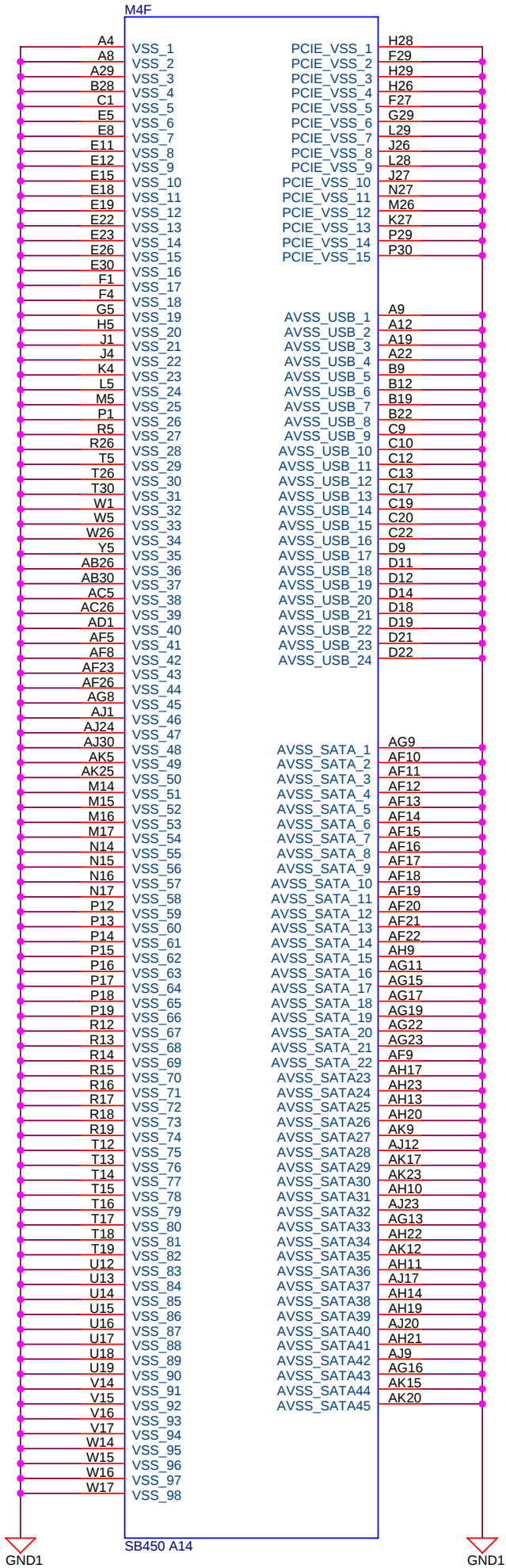
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									DRAW. No.		CAST
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Dolphin

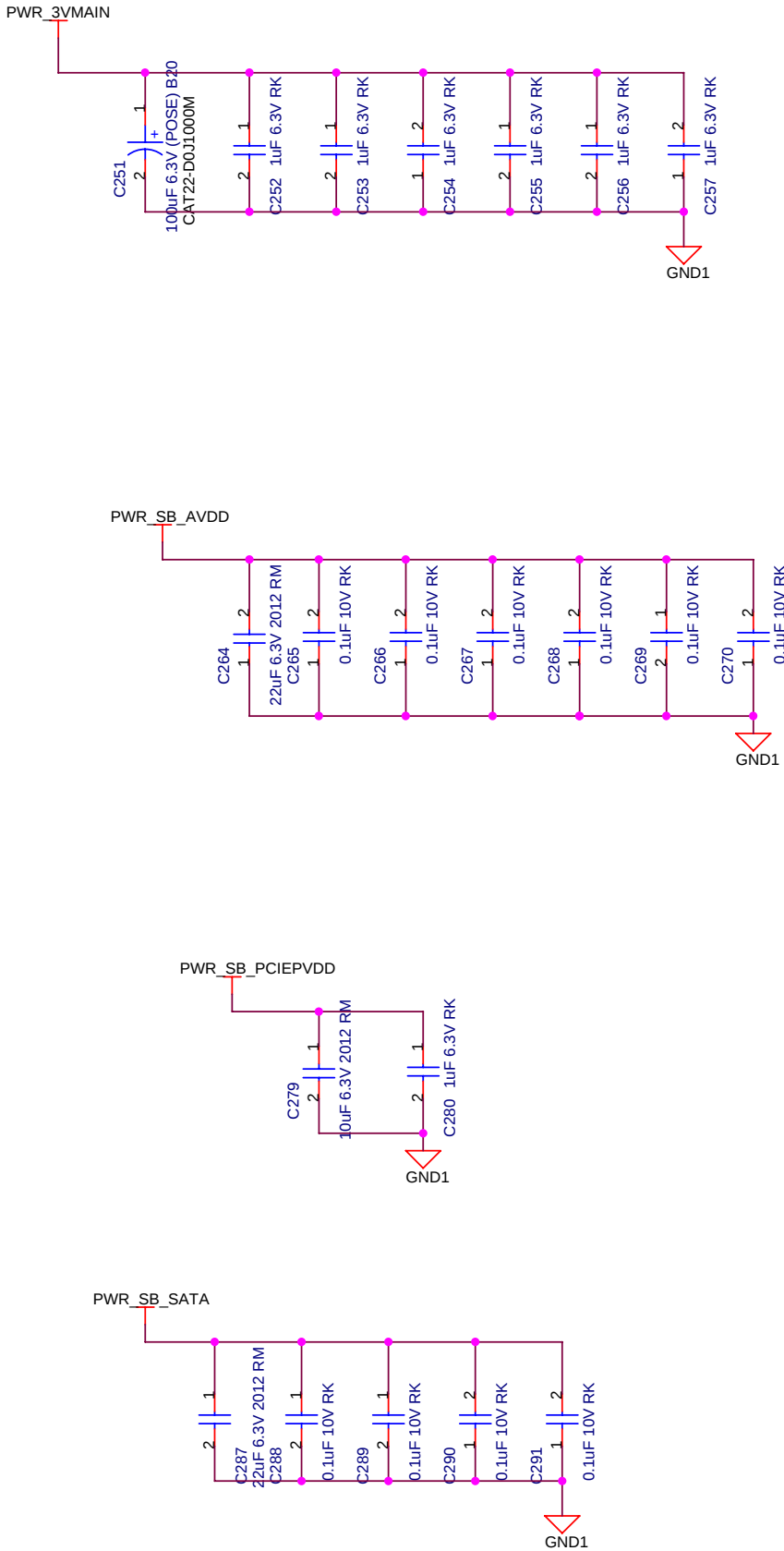
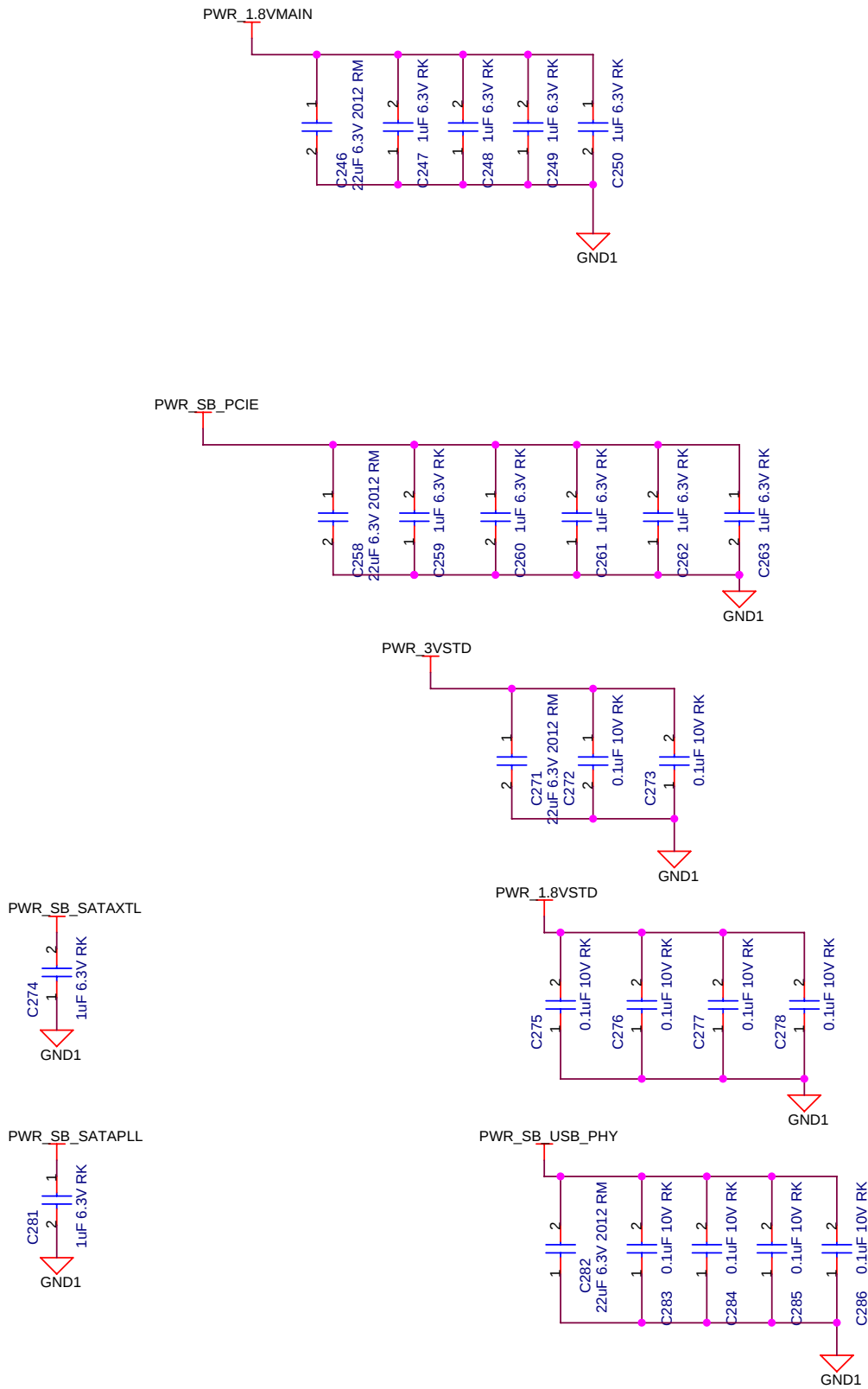
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SB450-6

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						VB313AA		
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

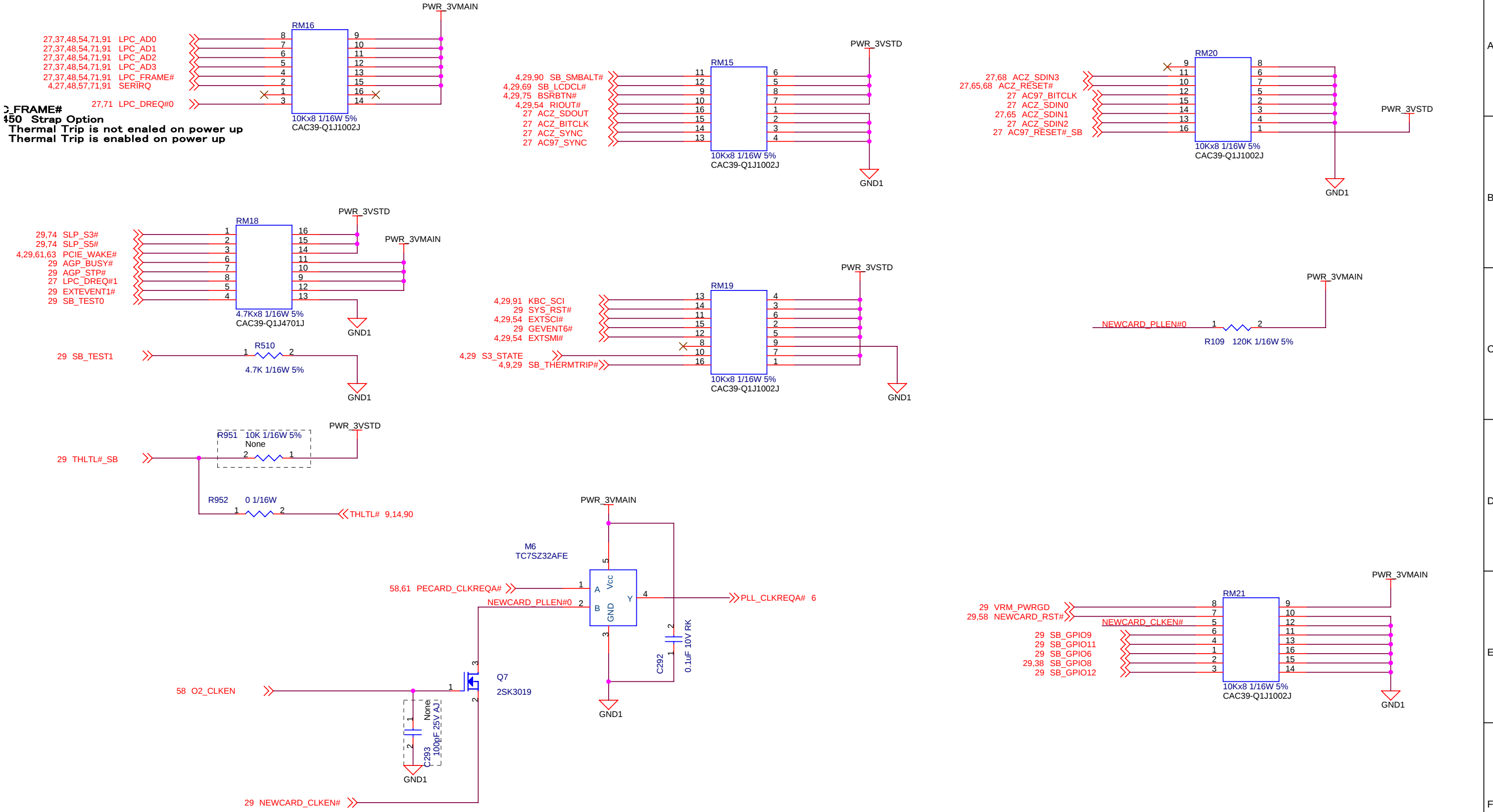


これらのパスコンはSB450近傍、可能な限りピンの直近に配置願います

SB450-7

						TITLE	
						VB313AA	
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						C1CP302570-X2	
						CAST	
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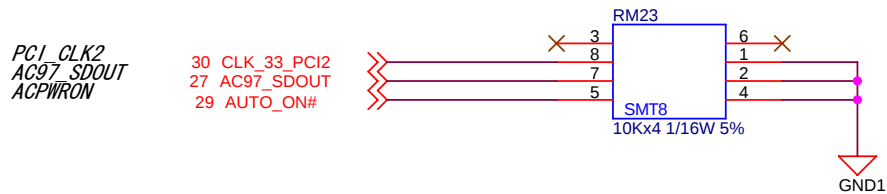
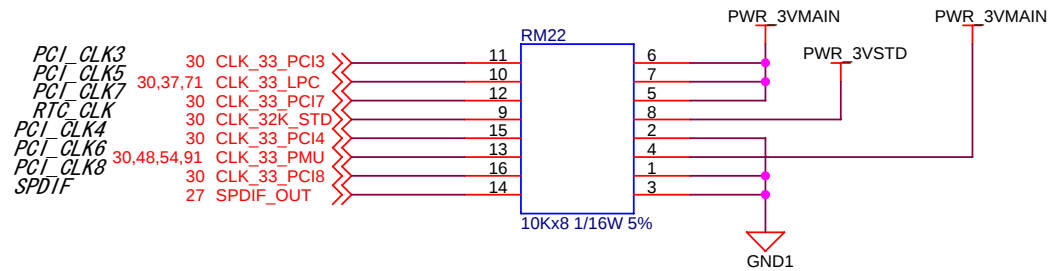
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04/28
部品削除 : R494, R495, R787, R788

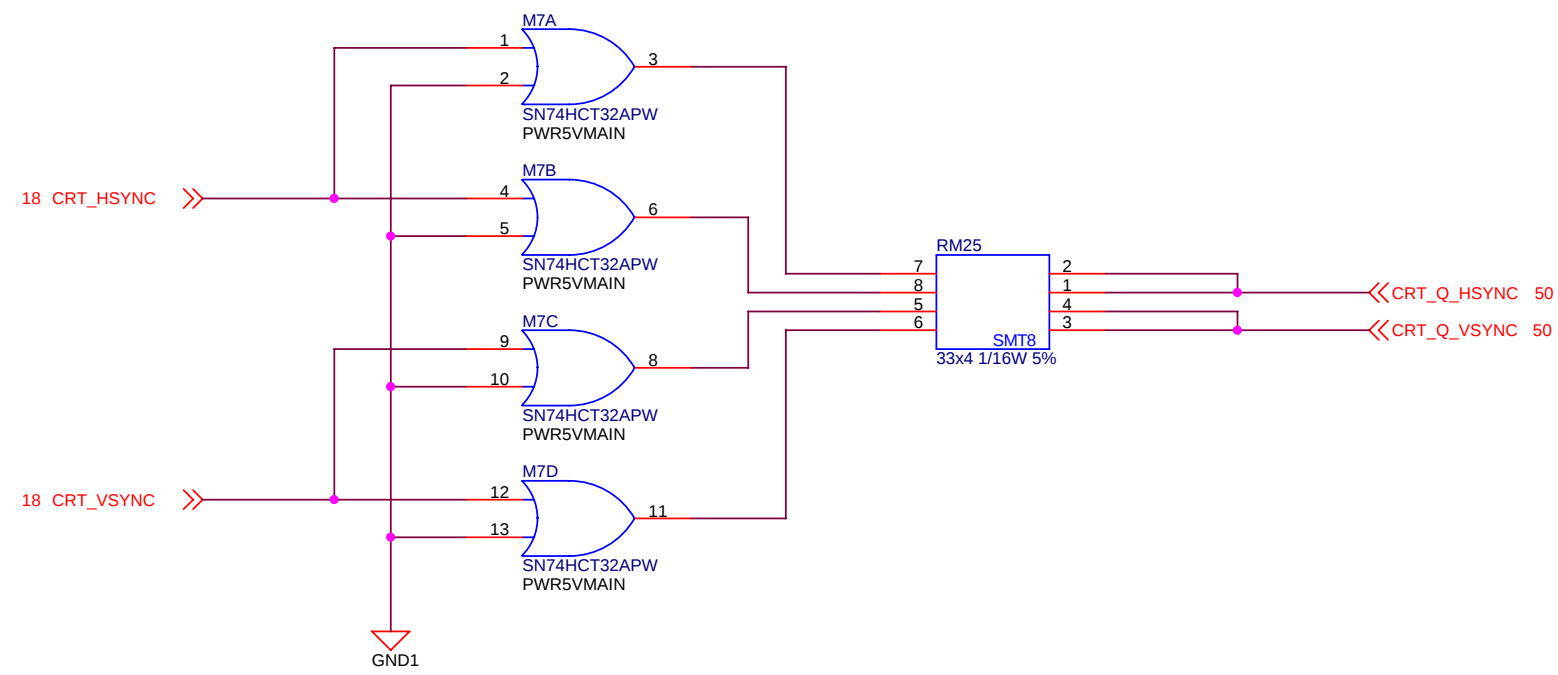
SB450 Pull Up/Down

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Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD.
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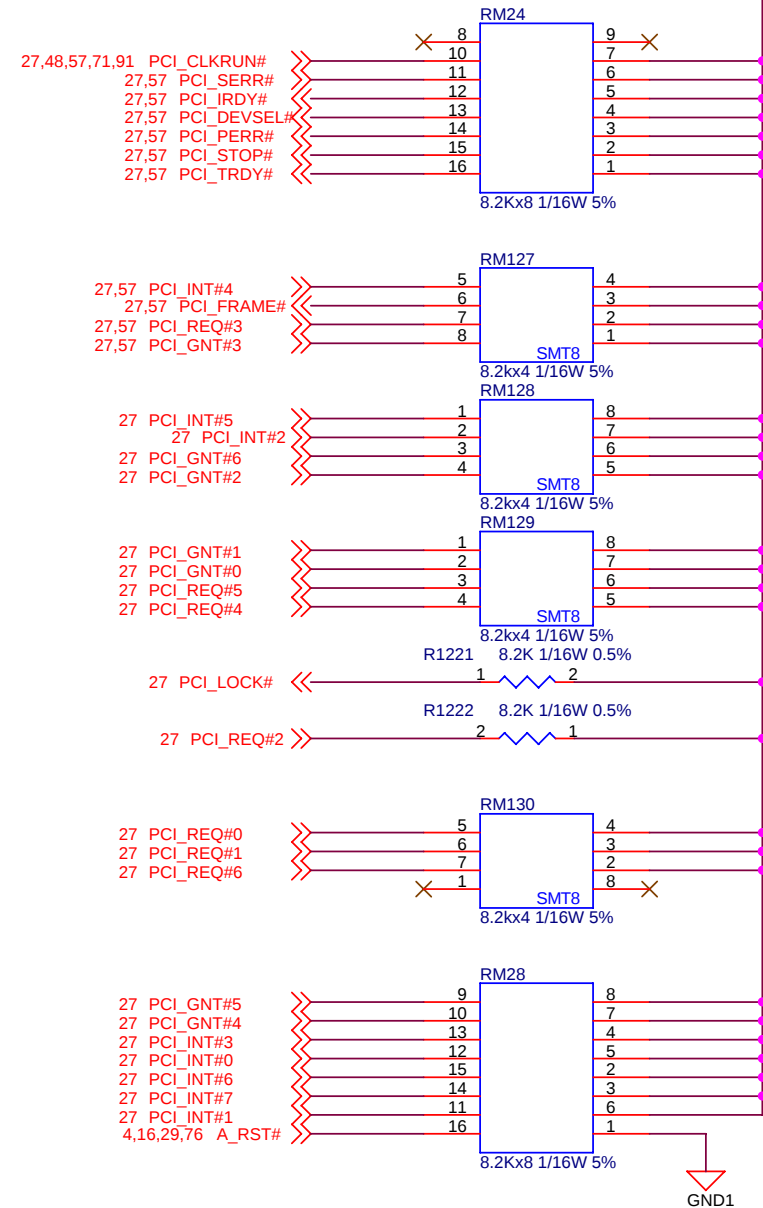
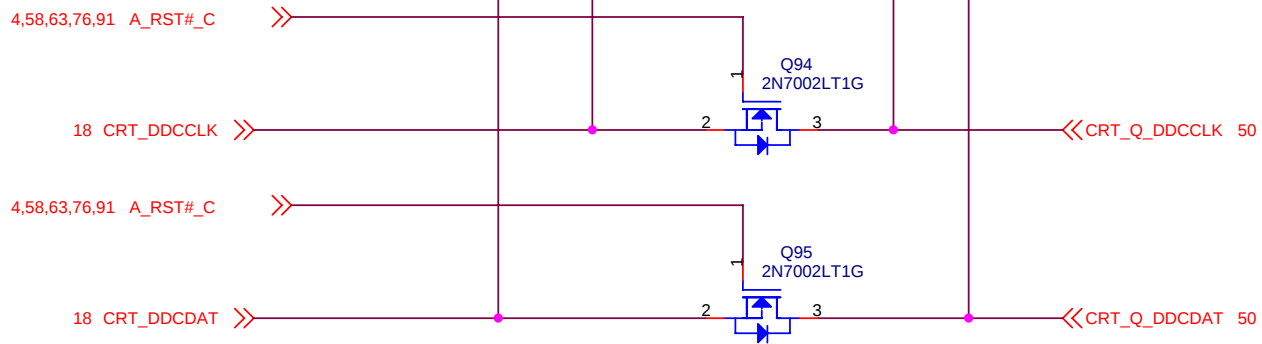
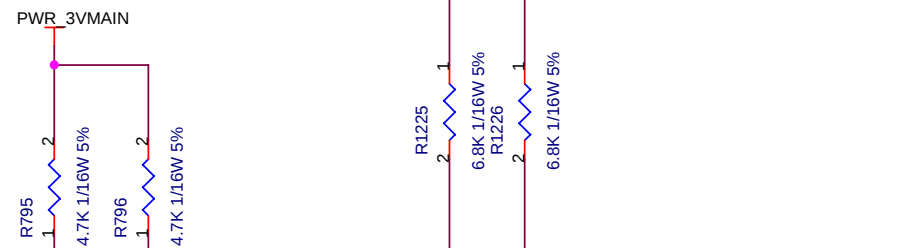
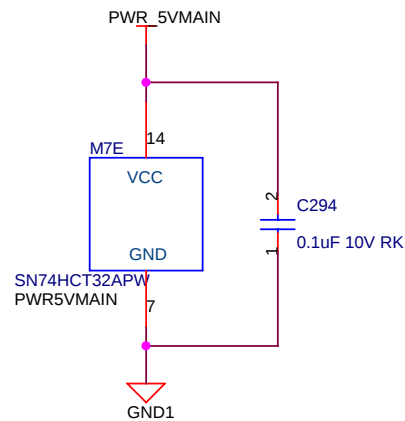


Pin Name	Description					Post-Beira Setting
ACPWRON	Active Manual Power On. 0 : Automatic Power On 1 : Manual Power On					0
AC97SDOUT	Enable/Disable additional straps for Debugging. 0 : Use Hardcoded defaults for Debug straps 1 : Enable additional Debug Strap					0
SPDIF	Select Speed for Super I/O. 0 : SIO Speed is 48MHz 1 : SIO Speed is 24MHz					0
PCICLK7 PCICLK8	ROM Type Select					1
	PCICLK7	1	1	0	0	
	PCICLK8	0	1	0	1	0
ROM Type		LPC ROM (256K)	BIOS ROM (X-bus)	FWH	LPC ROM (512K/1M)	
PCICLK6	Define Type of CPU 0 : Intel Processors 1 : AMD K8					1
PCICLK5	48MHz Clock Pad Select 0 : Ctystal Pad 1 : Clock Input Buffer					1
PCICLK4	Bypsd USB PLL 0 : use external 48MHz 1 : use internal USB					0
PCICLK3	USB PHY Down 0 : Enable 1 : Disable					1
PCICLK2	48MHz Clock Pad Select 0 : Clock Input Buffer 1 : Ctystal Pad					0
RTC_CLK	RTC Select 0 : External RTC 1 : Internal RTC					1
LFRAME#	Thermal Trip Strap 0 : Thermal Trip is not enabled on power up 1 : Thermal Trip is enabled on power up (default)					1

Pin Name	Description	
IDEPDack	Generate Short Reset 0 : Use Short Reset 1 : Use Long Reset	
PCI_AD31 PCI_AD30	Overcharge Pump control Bit	
PCI_AD29 PCI_AD28	PLL VCO control bits	
PCI_AD27	Bypass PCI PLL 0 : Use internal IDE PLL. Generated PCI CLK 1 : Bypass internal PCI PLL	
PCI_AD26	Bypass ACPI BCLK 0 : Use internal ACPI_BCLK 1 : Bypass ACPI_BCLK	
PCI_AD25	Bypass IDE Clock 0 : Use Internal IDE CLK 1 : Bypass Internal IDE	
PCI_AD24	BLK core strap from I2ROM enable 0 : Use default Value 1 : getting the value from I2C	
PCI_AD23	EPROM Reserved	



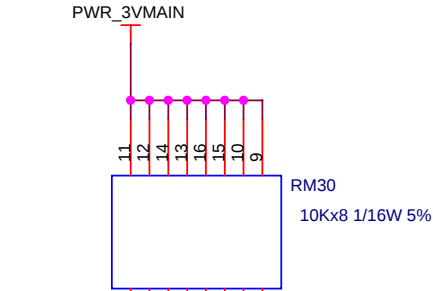
多連部品RM29については
配線しやすいようにピンスワップ可能。



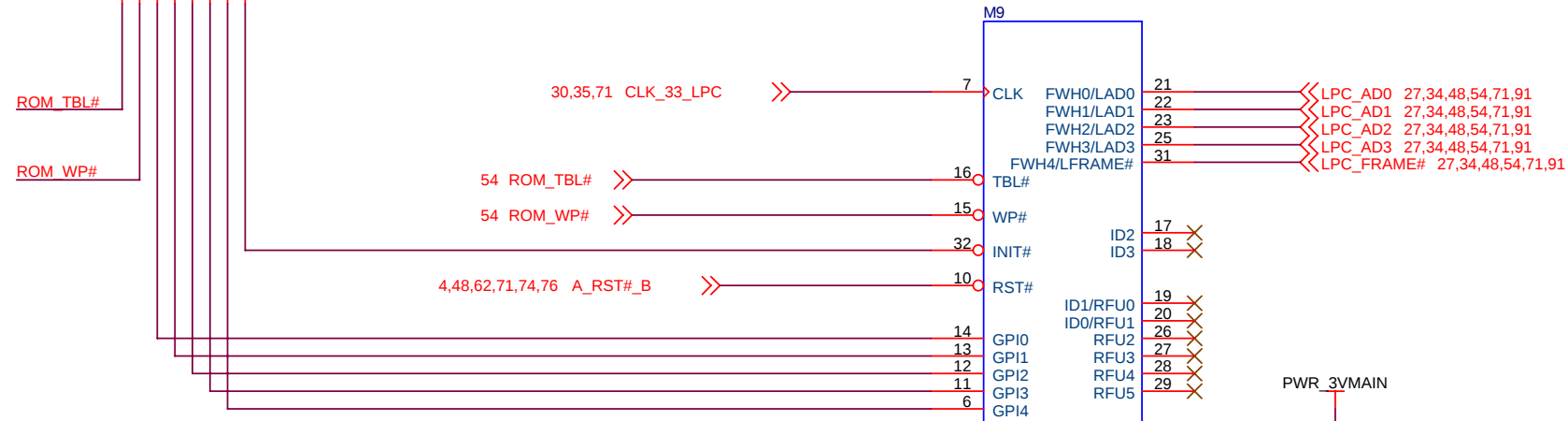
上記多連部品(8.2Kx4)については
配線しやすいようにピンスワップ可能。

Pullup for
AGP,PCI,LPC

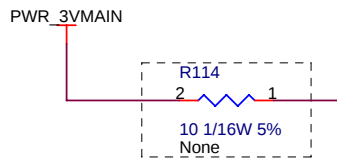
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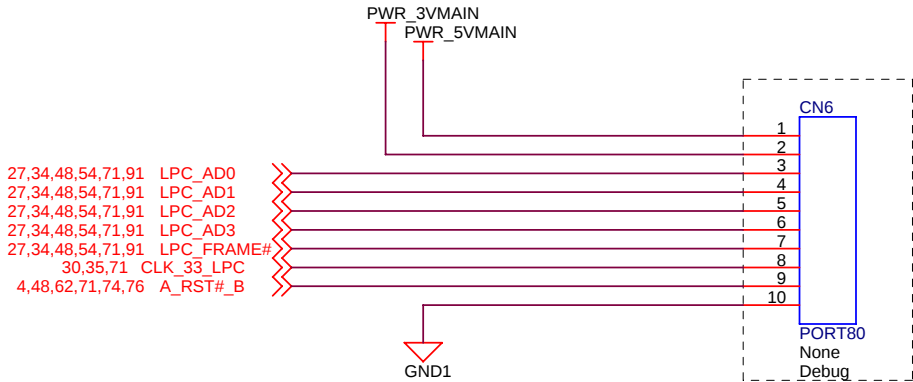
Socket for LPC ROM.
※LPC ROMはソケットを実装可能なパターンにすること。



M050FLW040 2pin has internal Pull-down

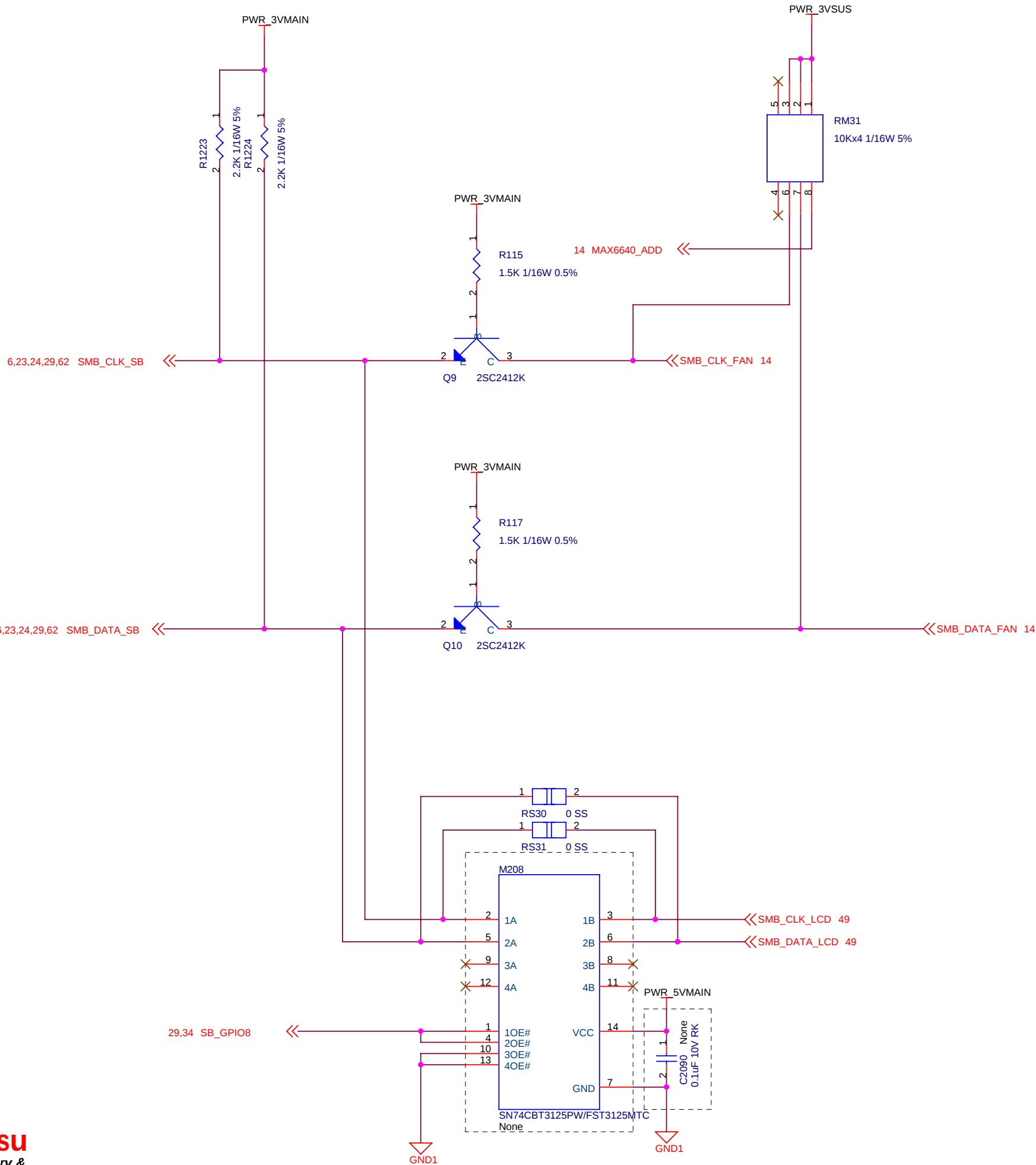


STM : 9pin PWR_3VMAIN
SST : 30pin
PWR_3VMAIN



LPC ROM

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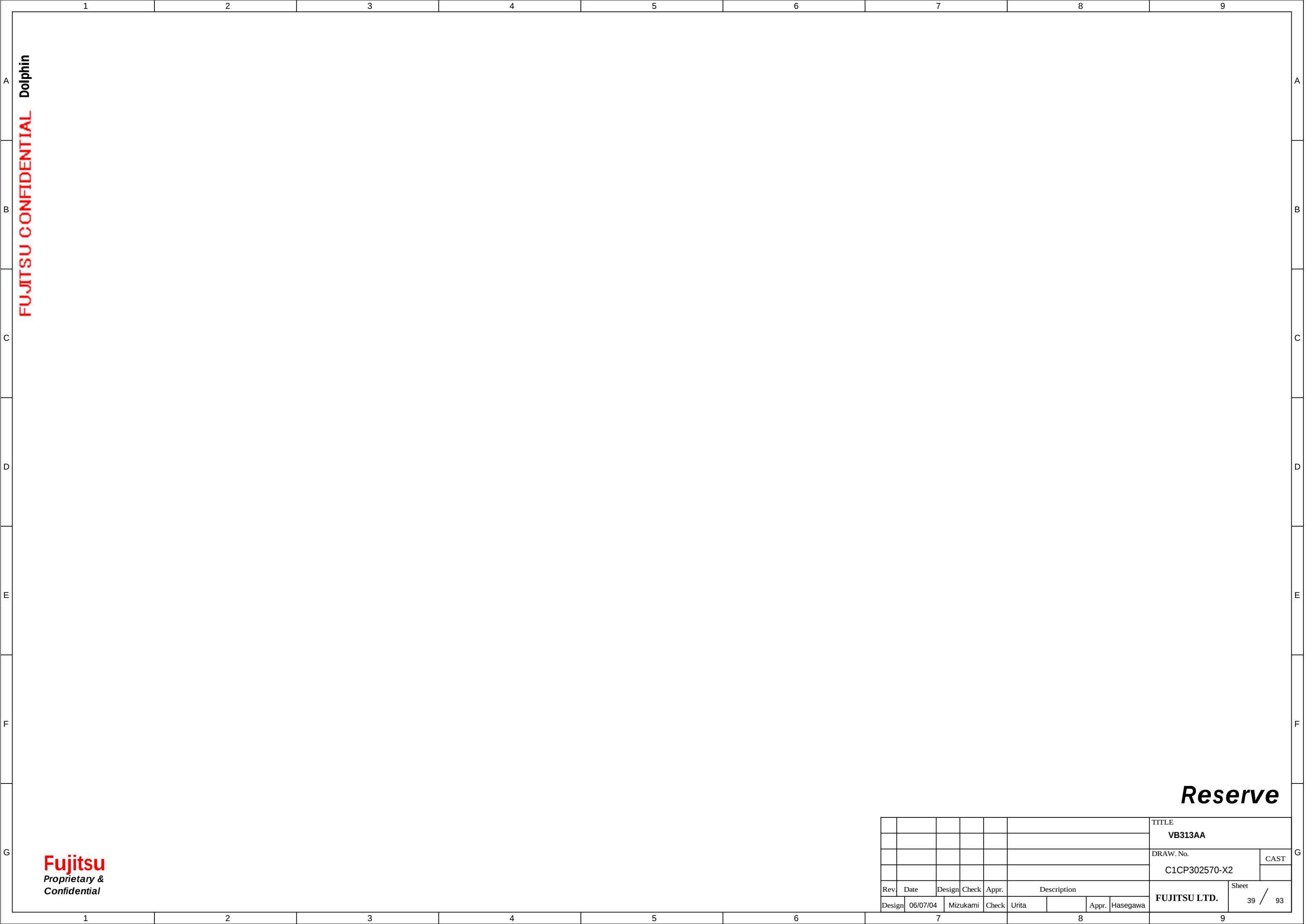


Device	Hex	Address
MAX6640	5Eh	0101 111x b
MEM slot0	A2h	1010 001x b
MEM slot1	A4h	1010 010x b
PMU	32h	0011 001x b
LCD(SPWG)	A0h	1010 000x b

BUS	Device	address
	DIMM1	A2h
	DIMM2	A4h
	MAX6640	5Eh
	LCD	A0h
PLL	PLL	D2h
PMU	PMU	32h

SMBus

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A	FUJITSU CONFIDENTIAL Dolphin							A
B								B
C								C
D								D
E								E
F								F
G								G
Fujitsu Proprietary & Confidential						Reserve		
1	2	3	4	5	6	7	8	9

					TITLE		
					VB313AA		
					DRAW. No.		CAST
					C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	43 / 93

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D																		D	
E																		E	
F																		F	
G																		G	

FUJITSU CONFIDENTIAL

Dolphin

Fujitsu

Proprietary & Confidential

Reserve

									TITLE				
									VB313AA				
									DRAW. No.		CAST		
									C1CP302570-X2				
Rev.	Date		Design	Check	Appr.	Description				FUJITSU LTD.		Sheet	
Design	06/07/04		Mizukami	Check	Urita			Appr.	Hasegawa	44 / 93			

1

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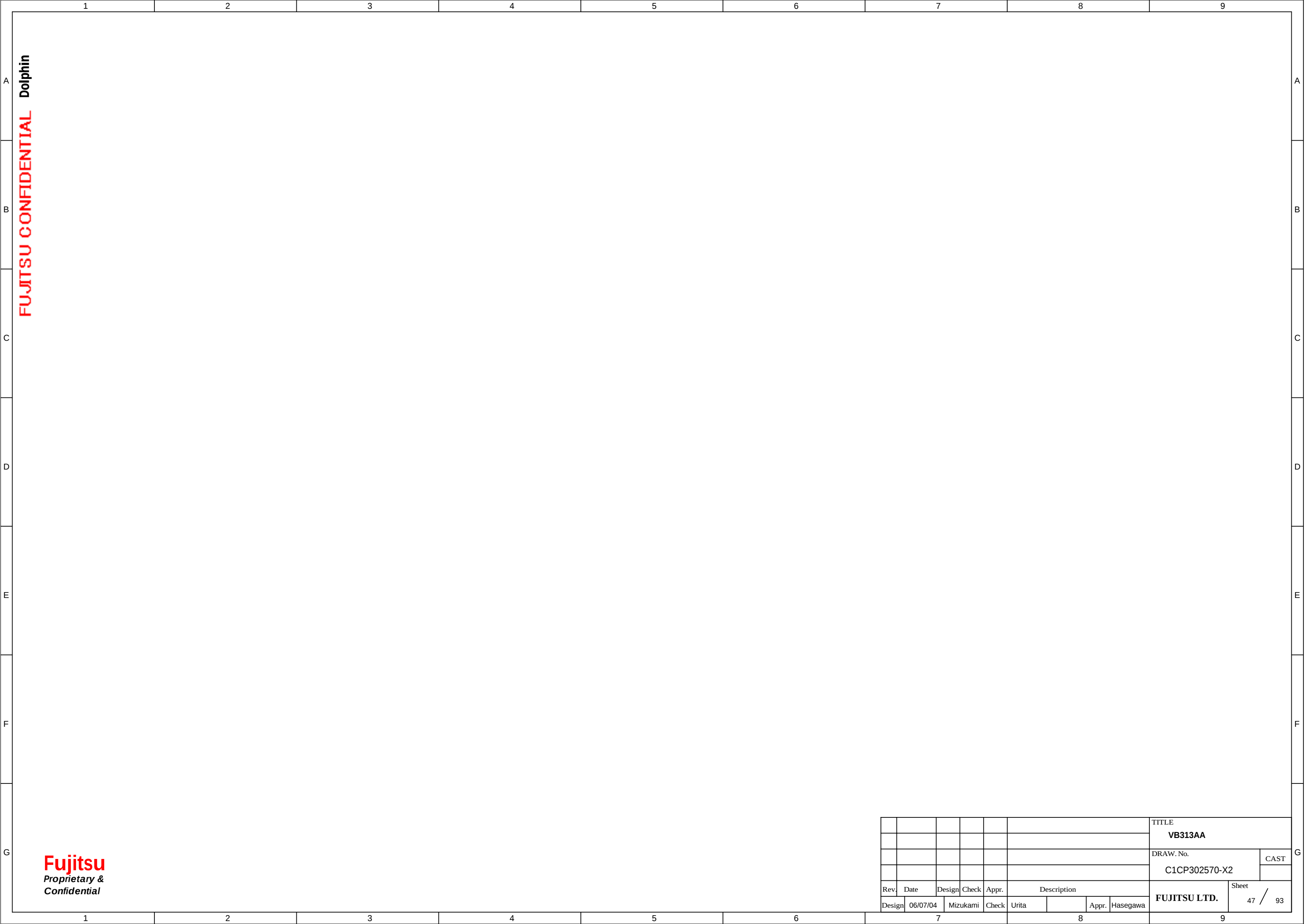
7

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FUJITSU CONFIDENTIAL

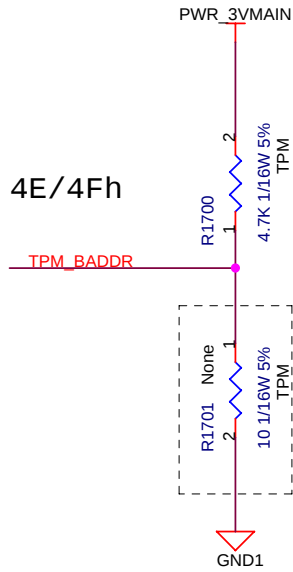
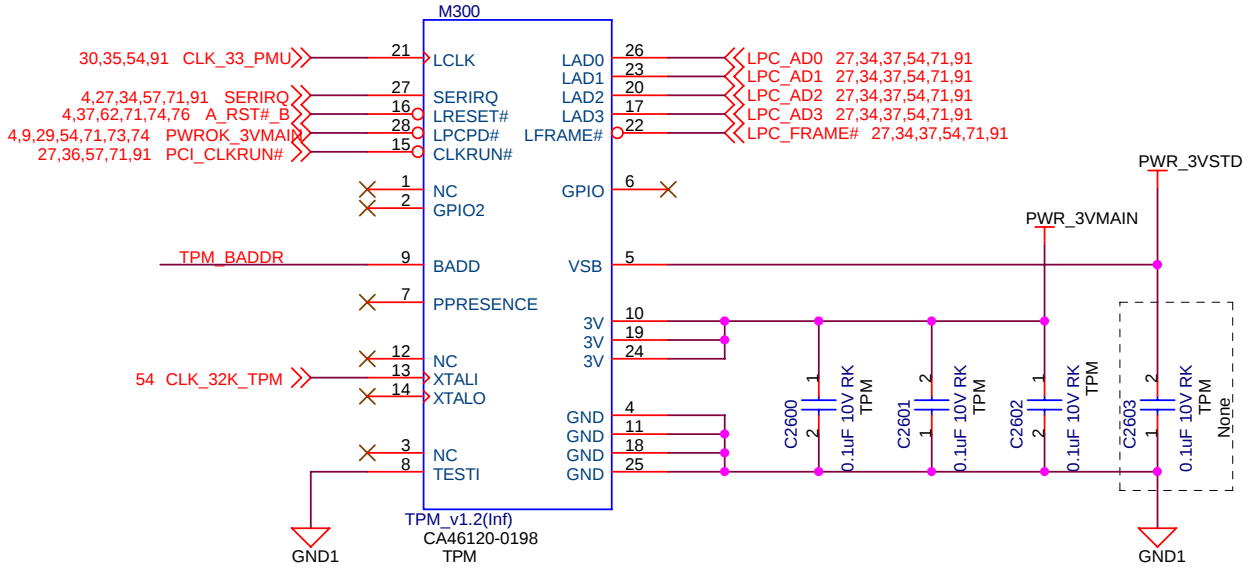
Dolphin

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						TITLE			
						VB313AA			
						DRAW. No.			CAST
						C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Fujitsu Ltd.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	47 /	93

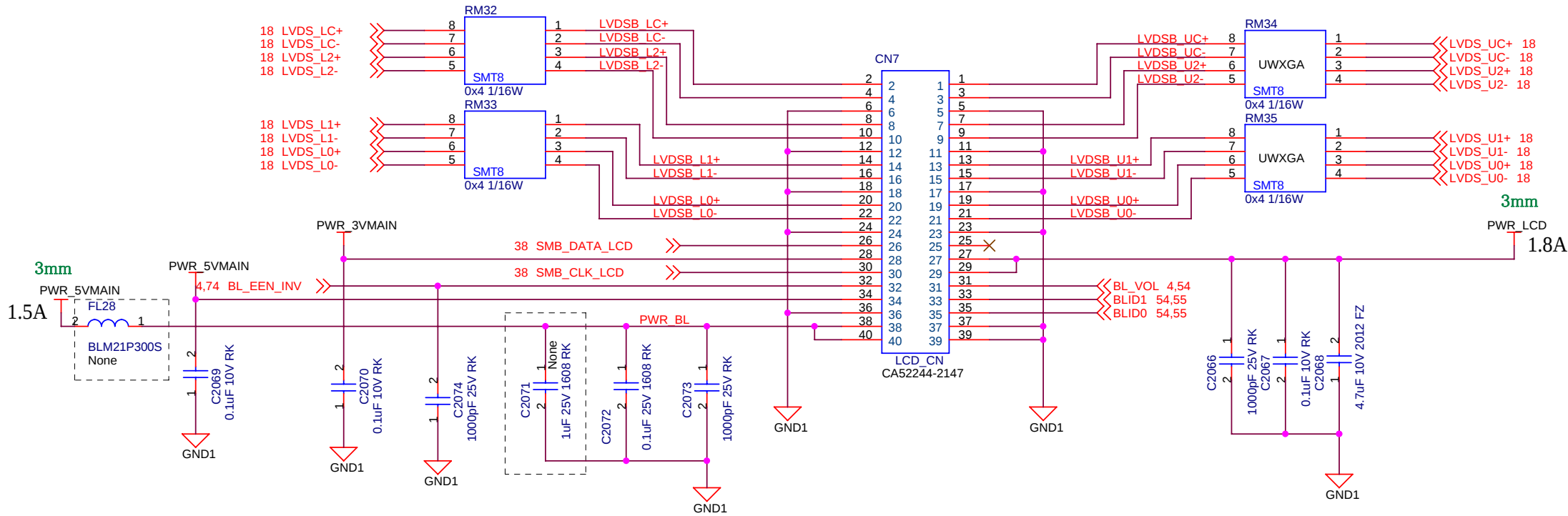
TPM Configuration

	High	Low
TPM_BADDR	4E/4Fh	2E/2Fh



TPM

						TITLE	
						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	48 / 93



各LVDSのパターンから上記部品までの距離(スタブ) はできるだけ短くすること。
Stub of LVDS is shortest.

LVDxxの設計条件
-原則として等長配線する(各線長の誤差は15mm以下)
-LVDS0+, -とLVDS0+, -とLVDS1+, -とLVDS2+, -の間はGNDでガードする
-各線のインピーダンスを100Ωにする
-ビヤ打ちは最小限(3回以下)とし、各信号等長でピア打ちをすること

LCD CN

									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	49 / 93	

これらのコンデンサは可能な限りCN8直近に配置し、
GNDパターンは引き回さず、VIAでGND層に落とすこと。

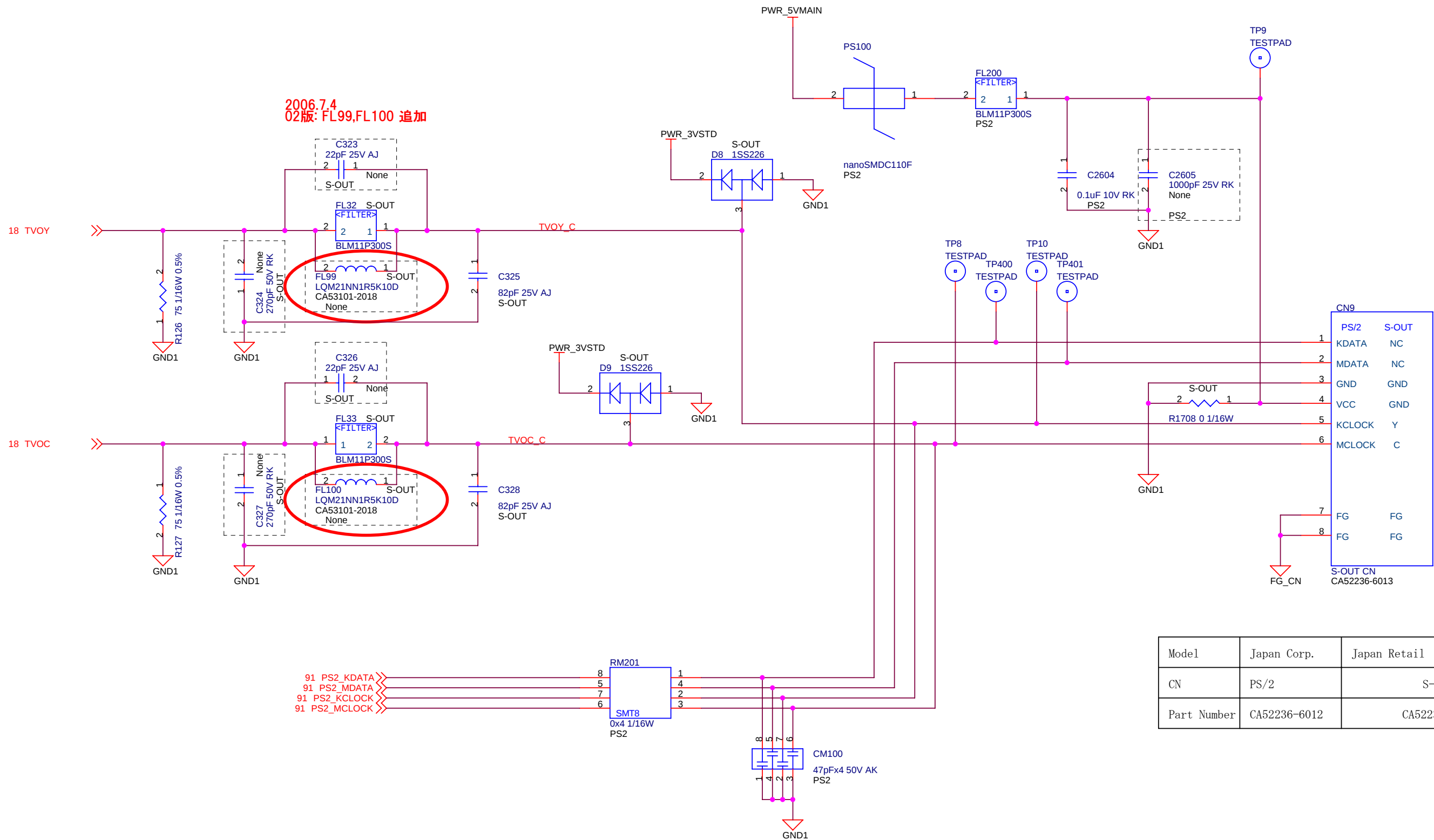
R119,120,121はCN7近傍に配置

これらのESD対策コンデンサは、
可能な限りDiodeの直近に配置すること

本ページに記載されている部品は
CRTコネクタの近くに配置すること。

CRT

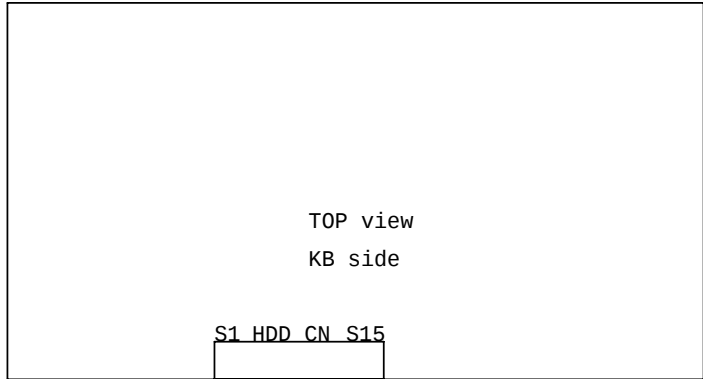
							TITLE	
							VB313AA	
							DRAW. No.	
							C1CP302570-X2	
							CAST	
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	FUJITSU LTD.	
							50 / 93	



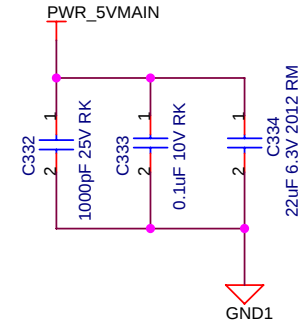
Model	Japan Corp.	Japan Retail Oversea
CN	PS/2	S-OUT
Part Number	CA52236-6012	CA52236-6013

S-OUT/PS2

									TITLE	
									VB313AA	
									DRAW. No.	CAST
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		51 / 93	

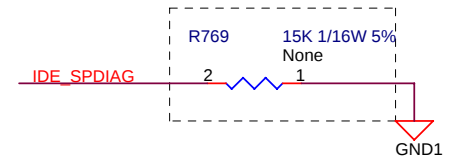
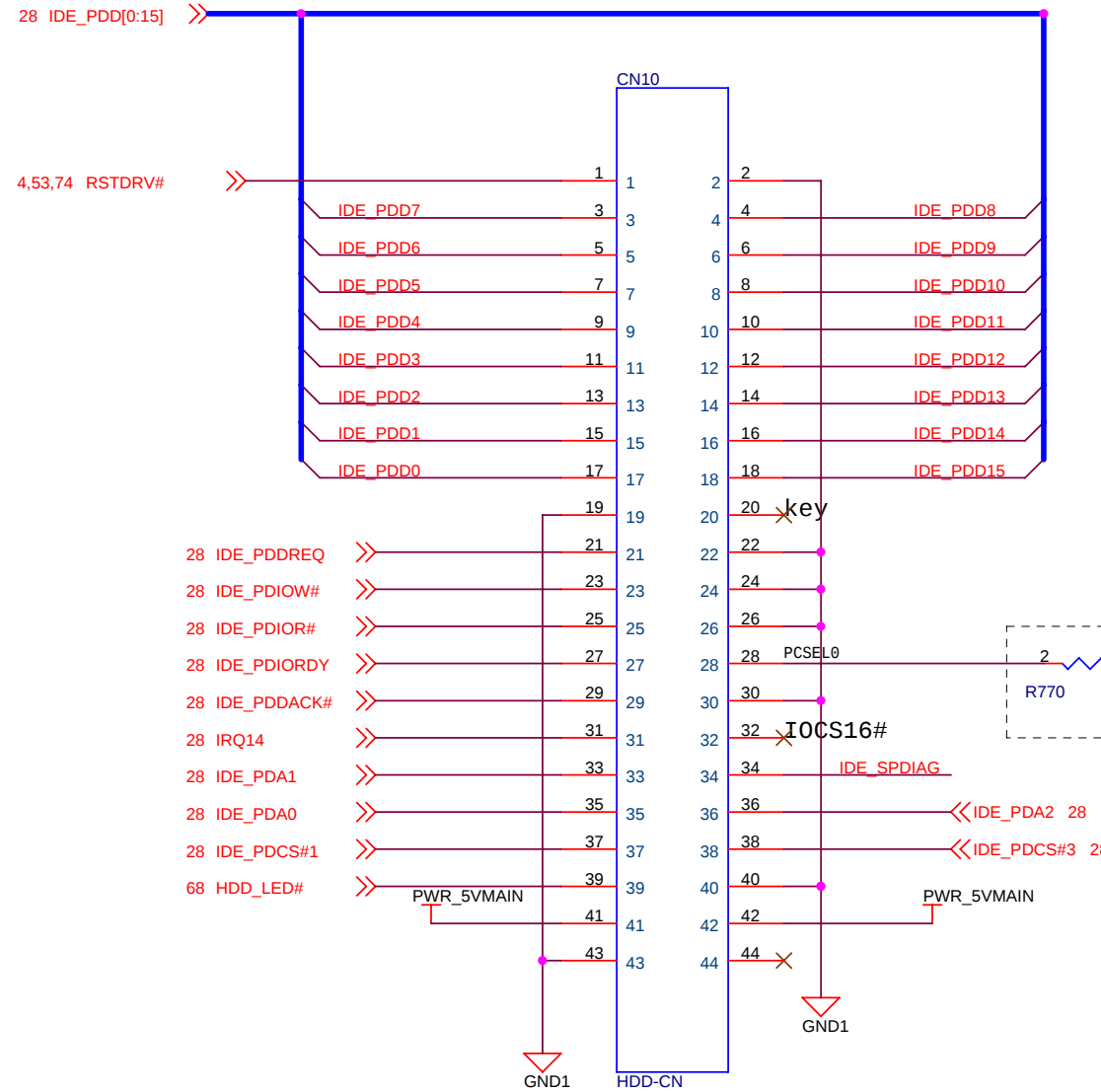


Max:2A
Supply enough current volume.
Need tie to GND1 fully.



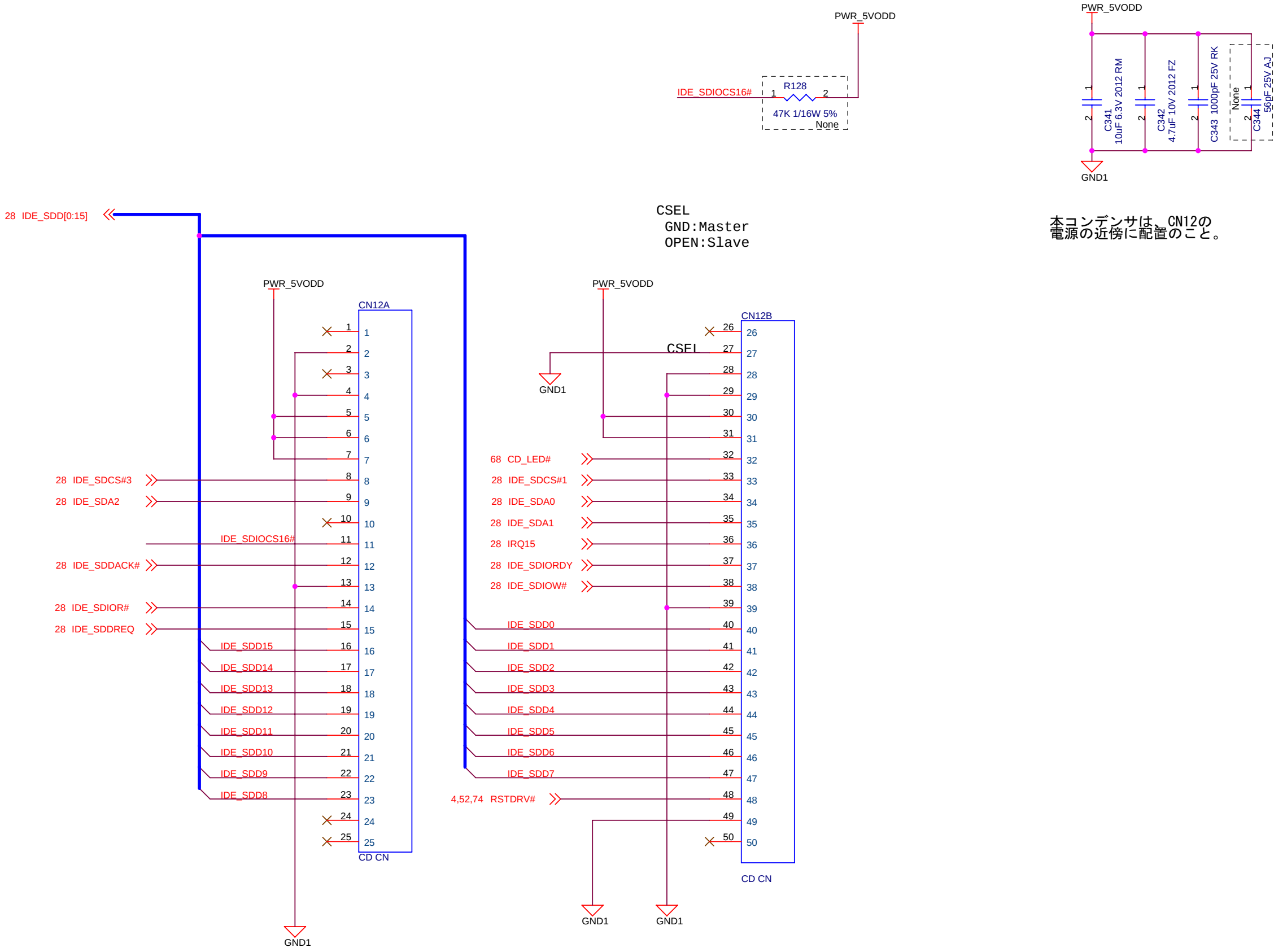
Place the capacitors near power pin of HDD CN

容量の小さいコンデンサを優先的にHDD-CNの電源PINの近くに配置すること。



1st HDD CN

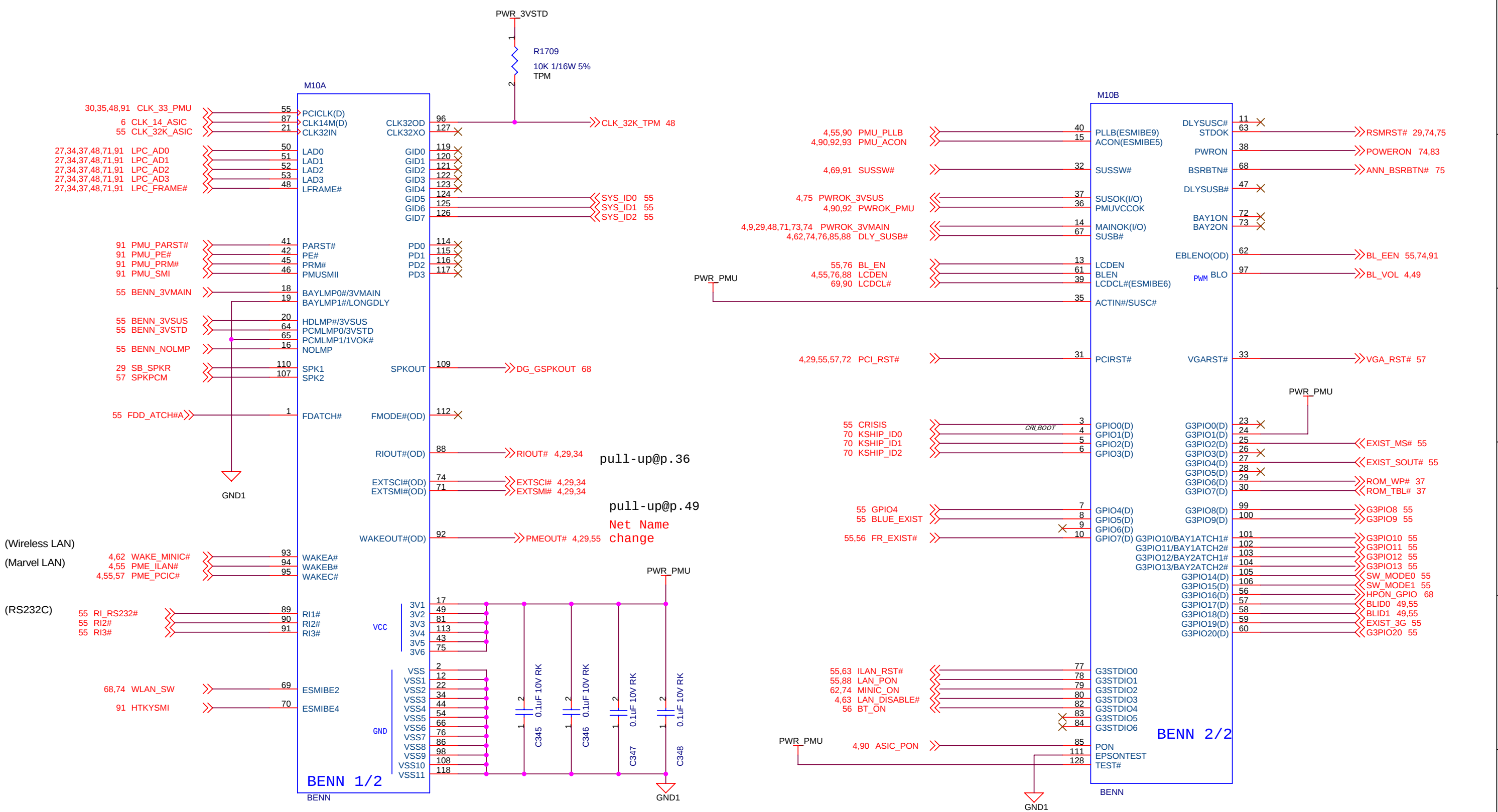
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Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		52 / 93	



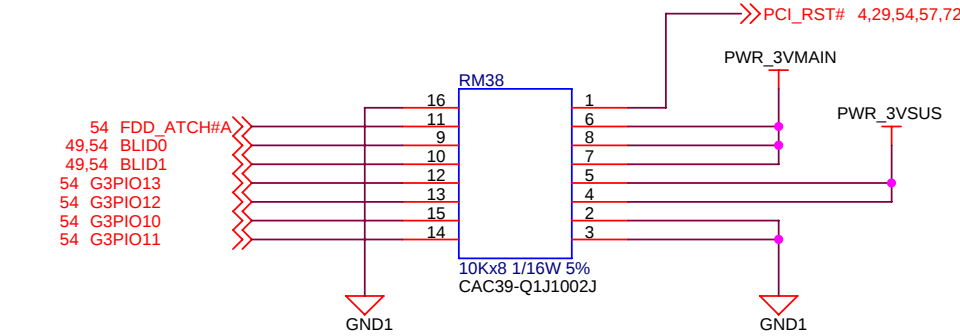
本コンデンサは、CN12の電源の近傍に配置のこと。

ODD-CN

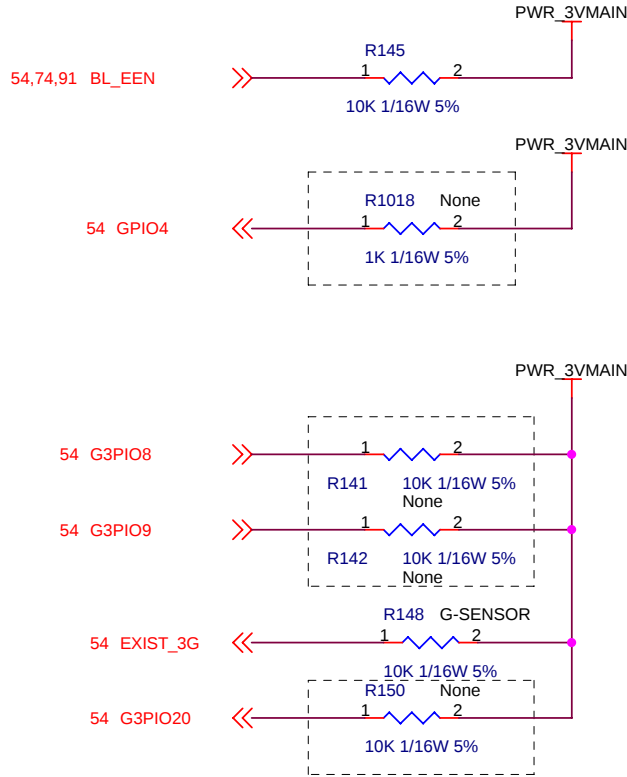
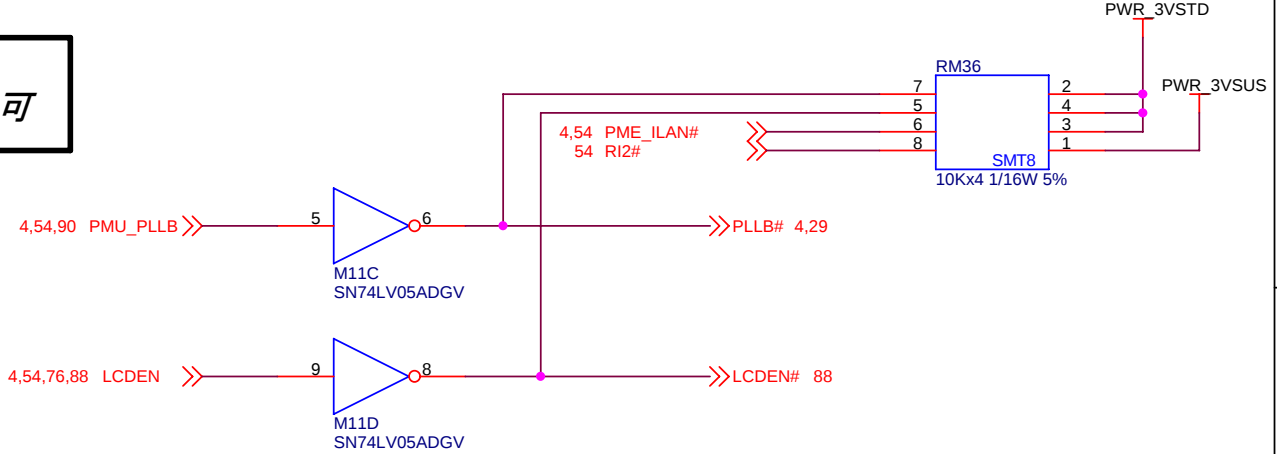
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						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	53 / 93



						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	54 / 93

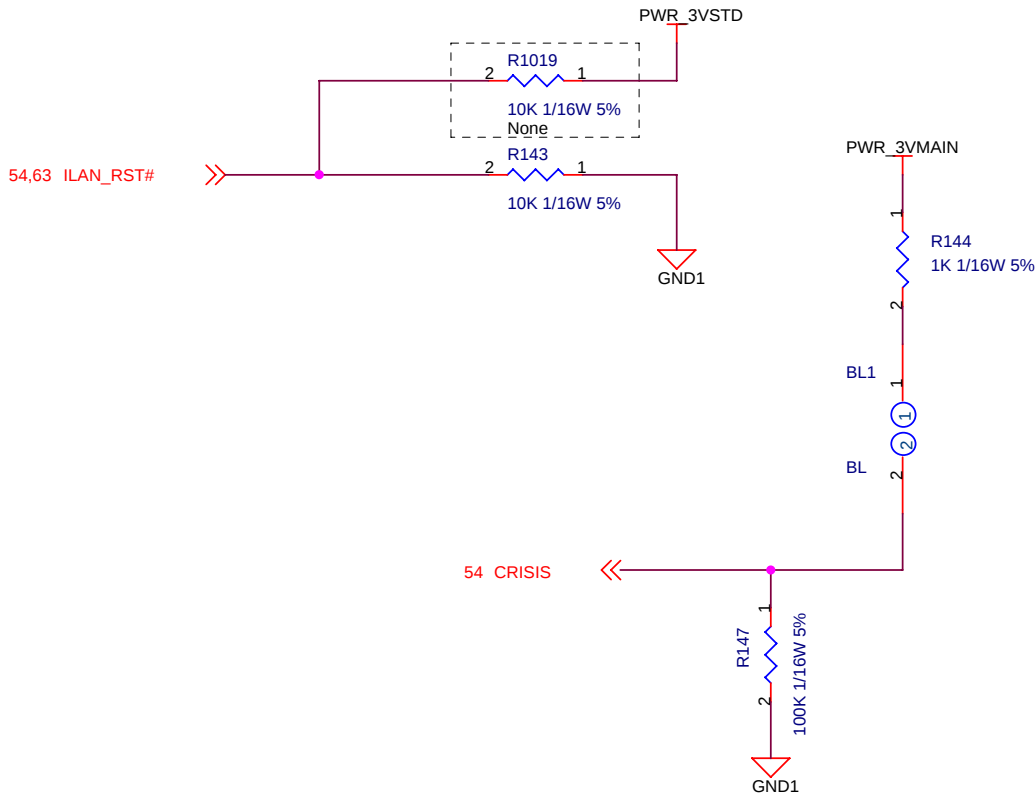
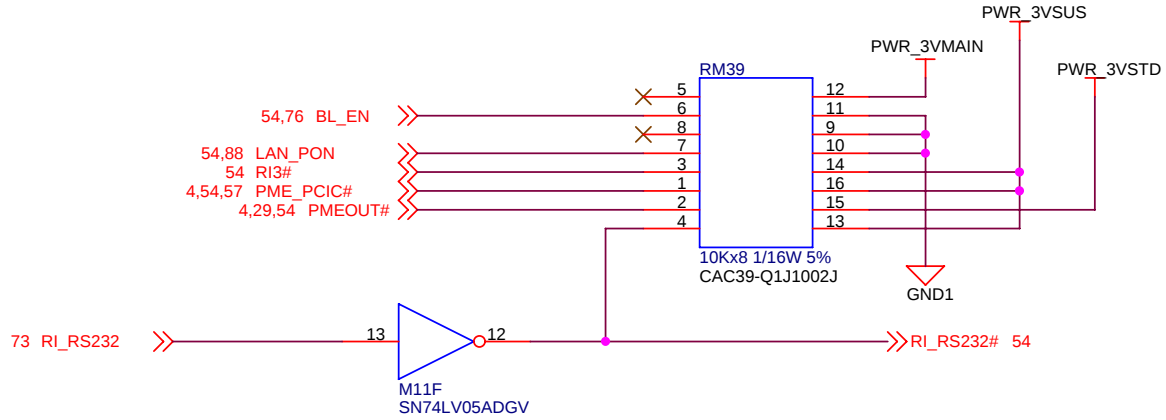


本ページ内の集合抵抗については、
同じ容量のものについては部品間PINSWAP可

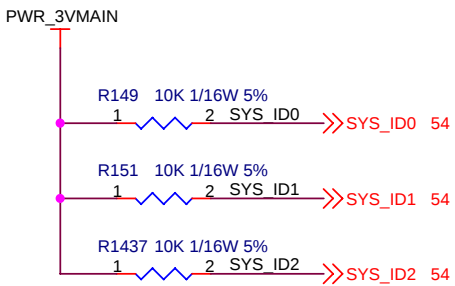


SW_MODE[1:0]
00 : 4ボタン(店頭/FCS)
[Appli], [Appli], [VolumeDown], [VolumeUp]
01 : 4ボタンモデル(FKL/FPC)
[Appli], [Appli], [Appli], [Appli]
10 : クラサバモデル
(T.B.D)
11 : 6ボタンモデル(仕向け先は未定。06秋冬はなし)
[Internet], [Mail], [A], [B], [VolumeDown], [VolumeUp]

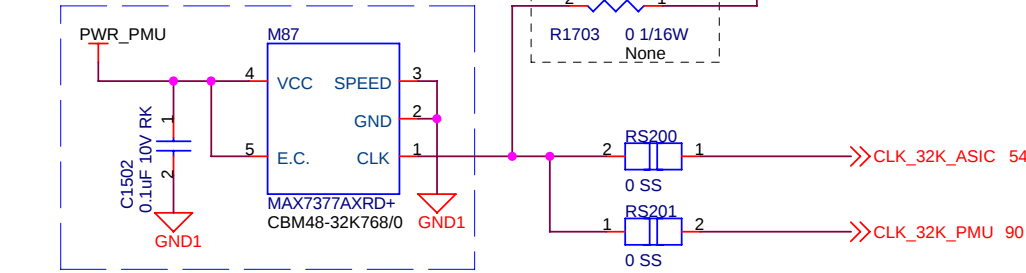
※本IC/CAPの外周、及びその直下層はGND1とする。
2個以上の貫通VIAでGND層へと接続すること。



Pullup/down
for BENN



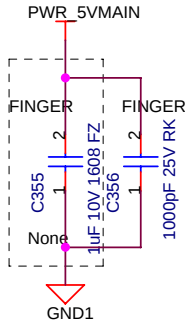
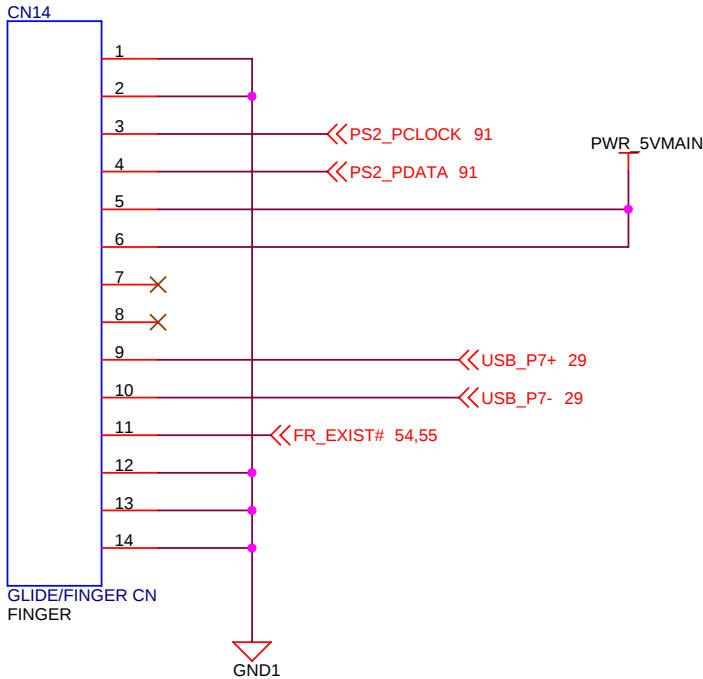
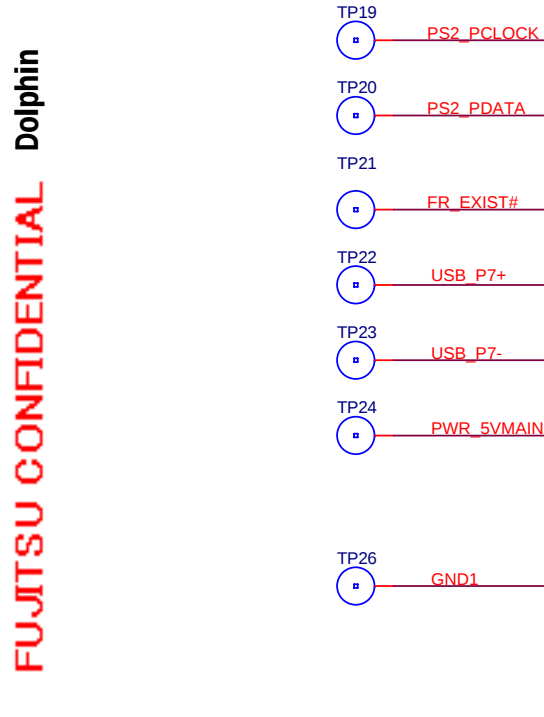
SYS_ID[2:0]
000 : 国内店頭
001 : 海外
010 : クラサバ
011 - 111 : Reserve



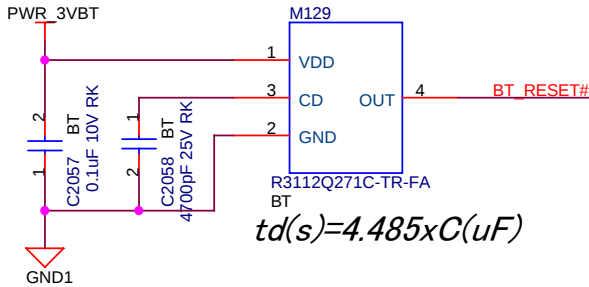
※本IC/CAPの外周、及びその直下層はGND1とする。
2個以上の貫通VIAでGND層へと接続すること。

本ページ内の集合抵抗については、
特に指定の無い限りBENNの近傍に配置すること。

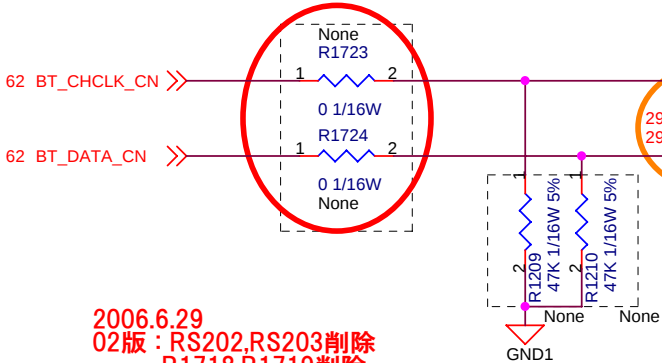
						TITLE	
						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa	55 / 93	
						FUJITSU LTD.	



Target 20ms



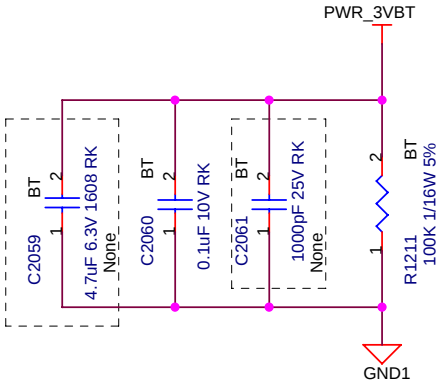
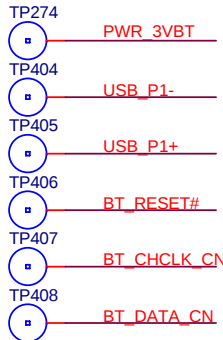
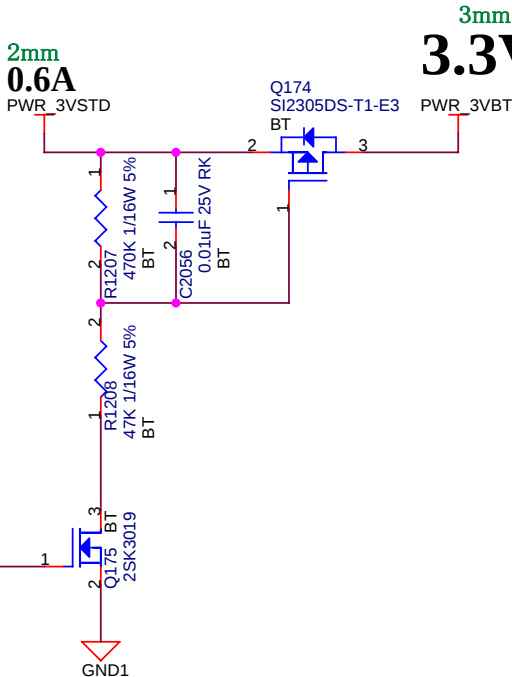
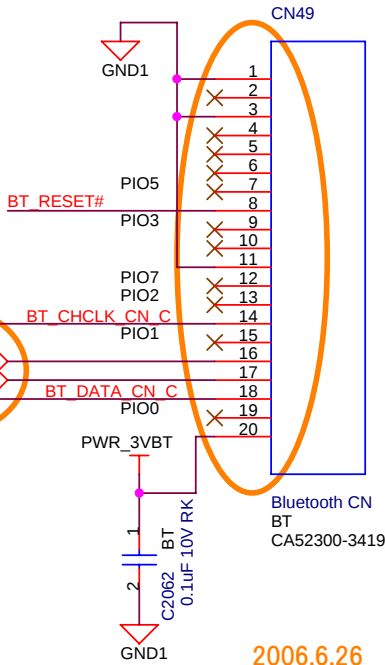
$td(s)=4.485 \times C(uF)$



2006.6.29
02版：RS202,RS203削除
R1718,R1719削除

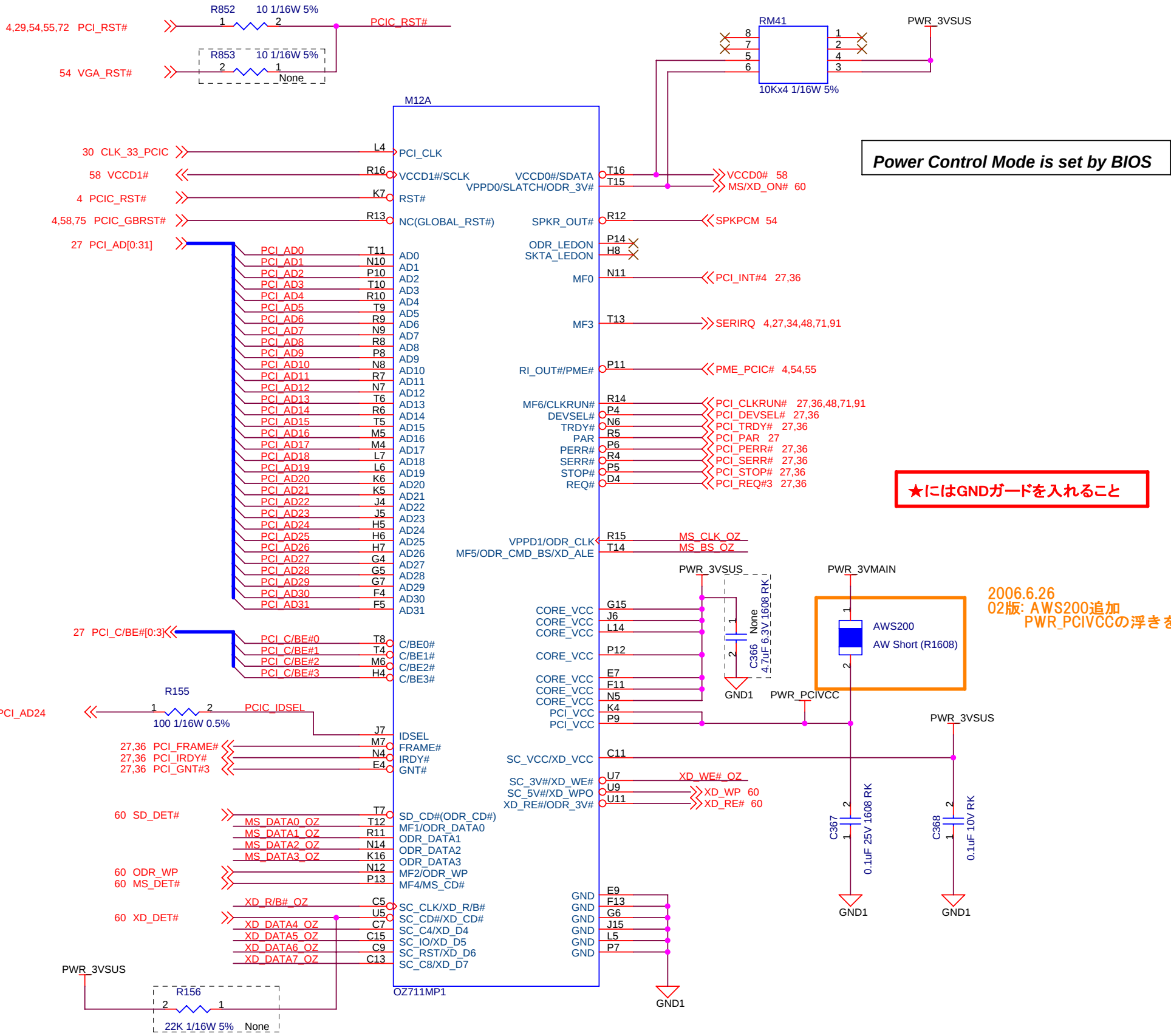
2006.6.26
02版：USB_P1+とUSB_P1-入れ替え

2006.6.26
02版：CN49のピンアサインを逆に変更

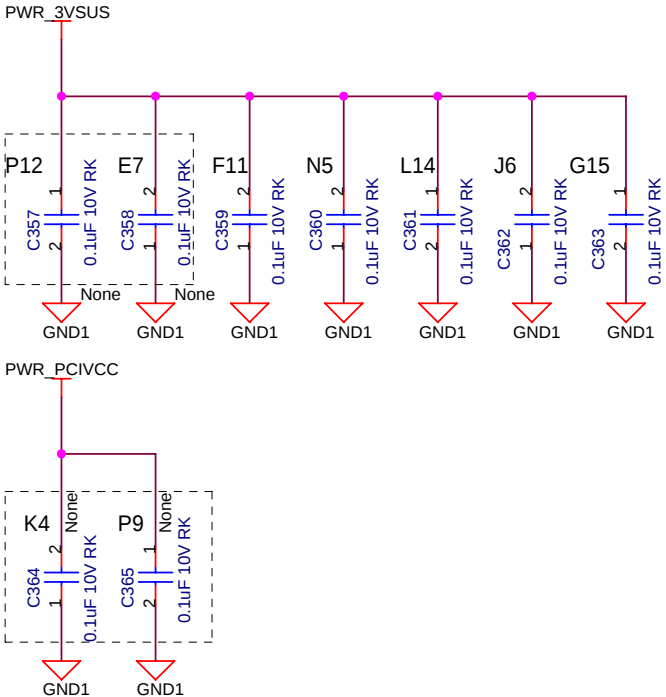


FINGER_CN

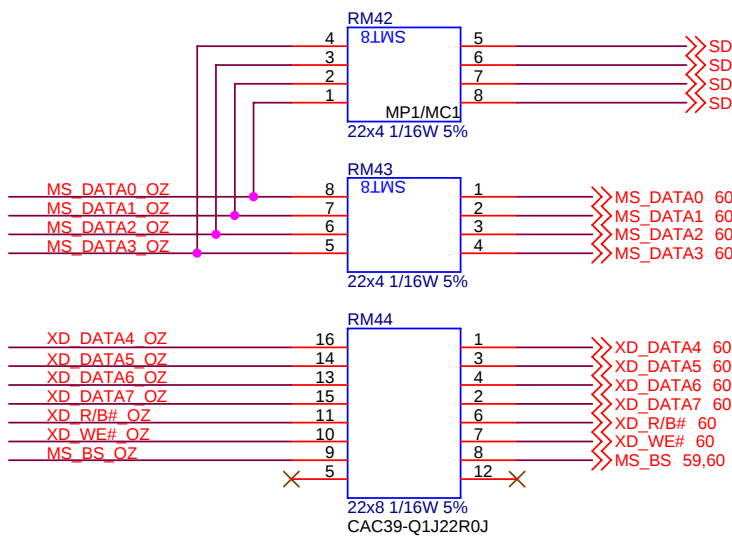
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						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	Sheet		
Design	06/07/04	Mizukami	Check	Urita		56 / 93		
						FUJITSU LTD.		



下記コンデンサは各電源PINの直近に配置すること。



2006.6.26
02版: AWS200追加
PWR_PCIVCCの浮きを修正

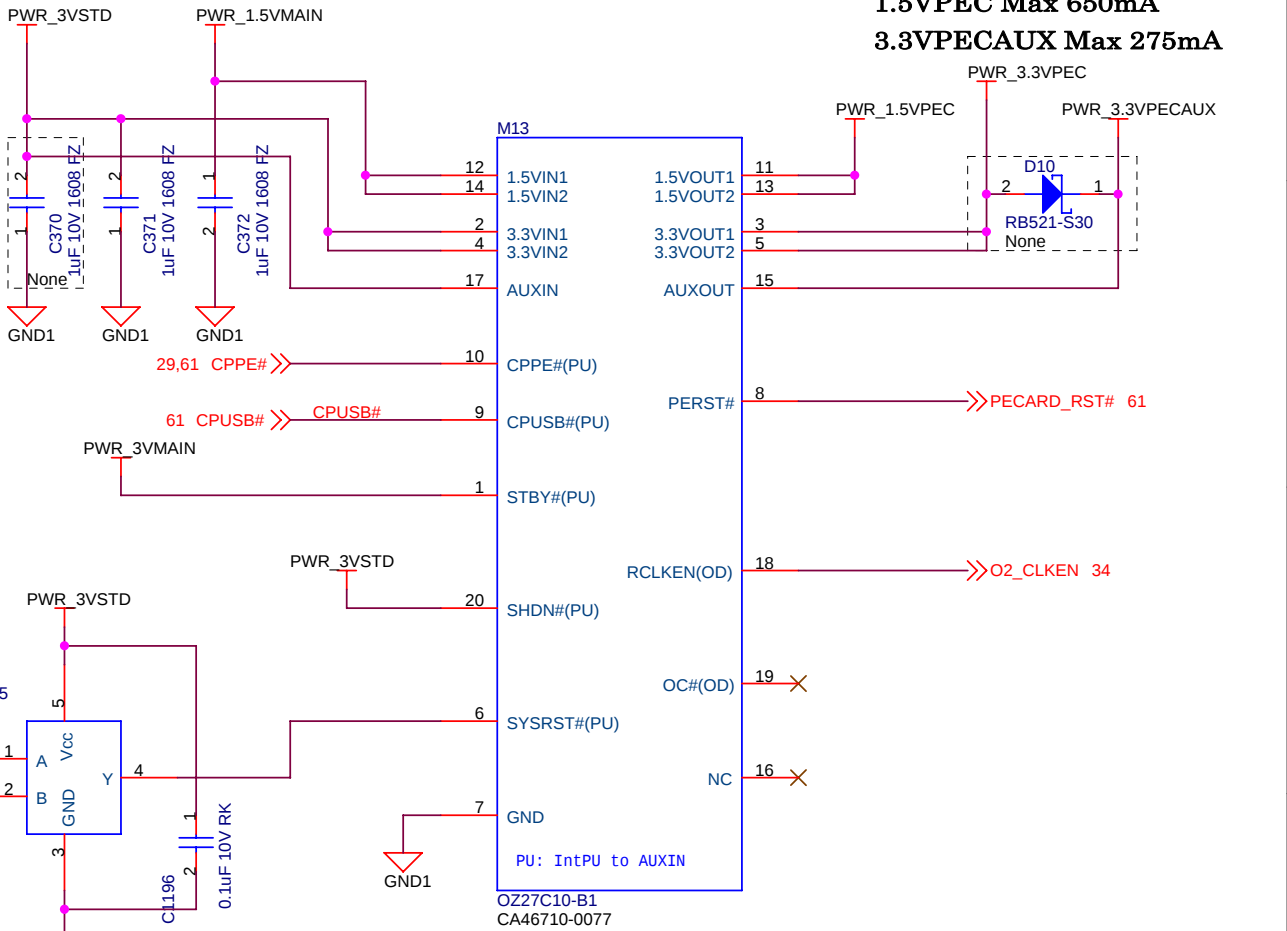
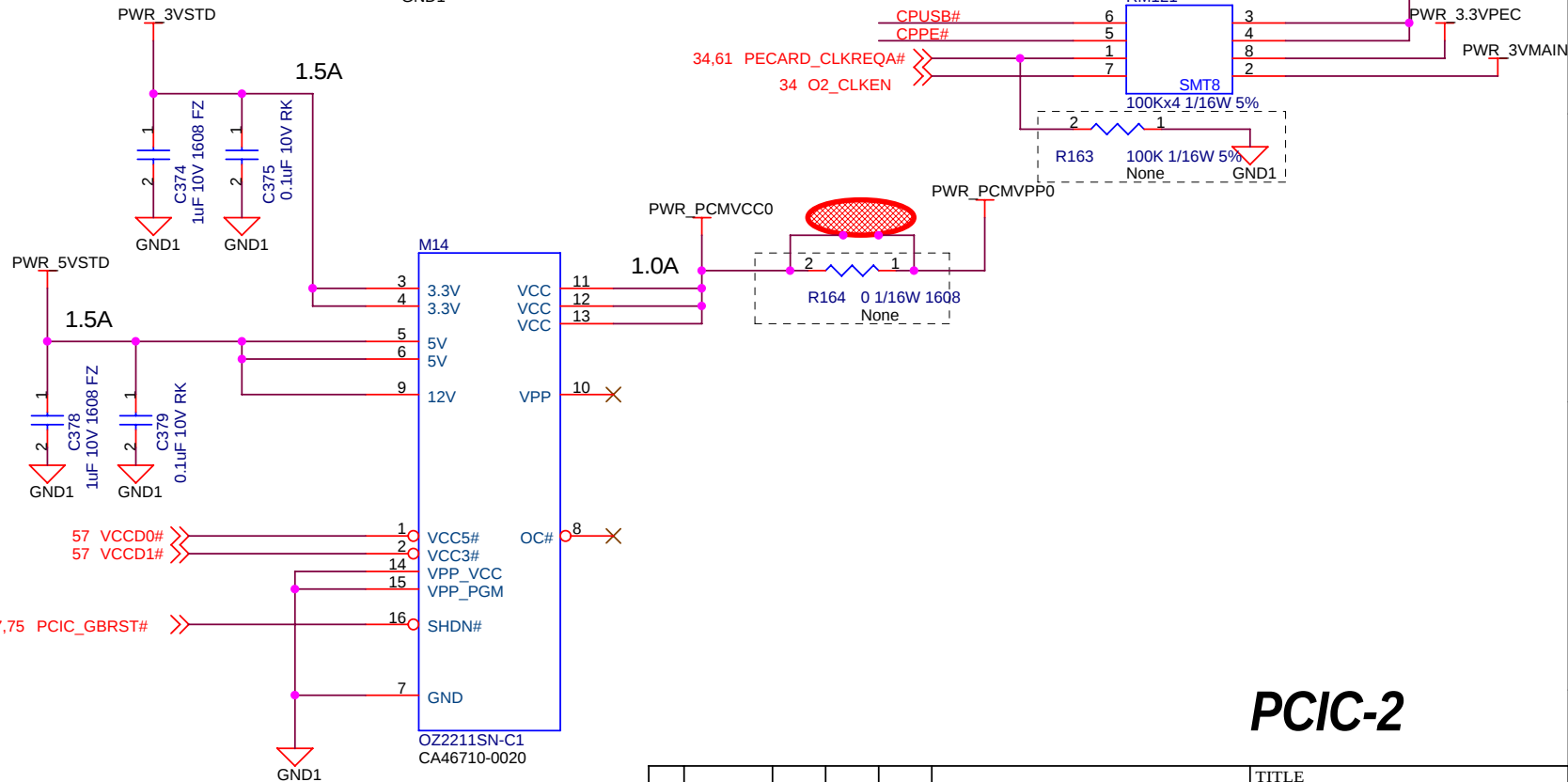
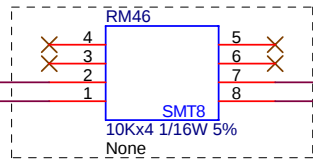


PCIC-1

♪はGND1で両端をガードすること

						TITLE			
						VB313AA			
						DRAW. No.		CAST	
						C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		57 / 93

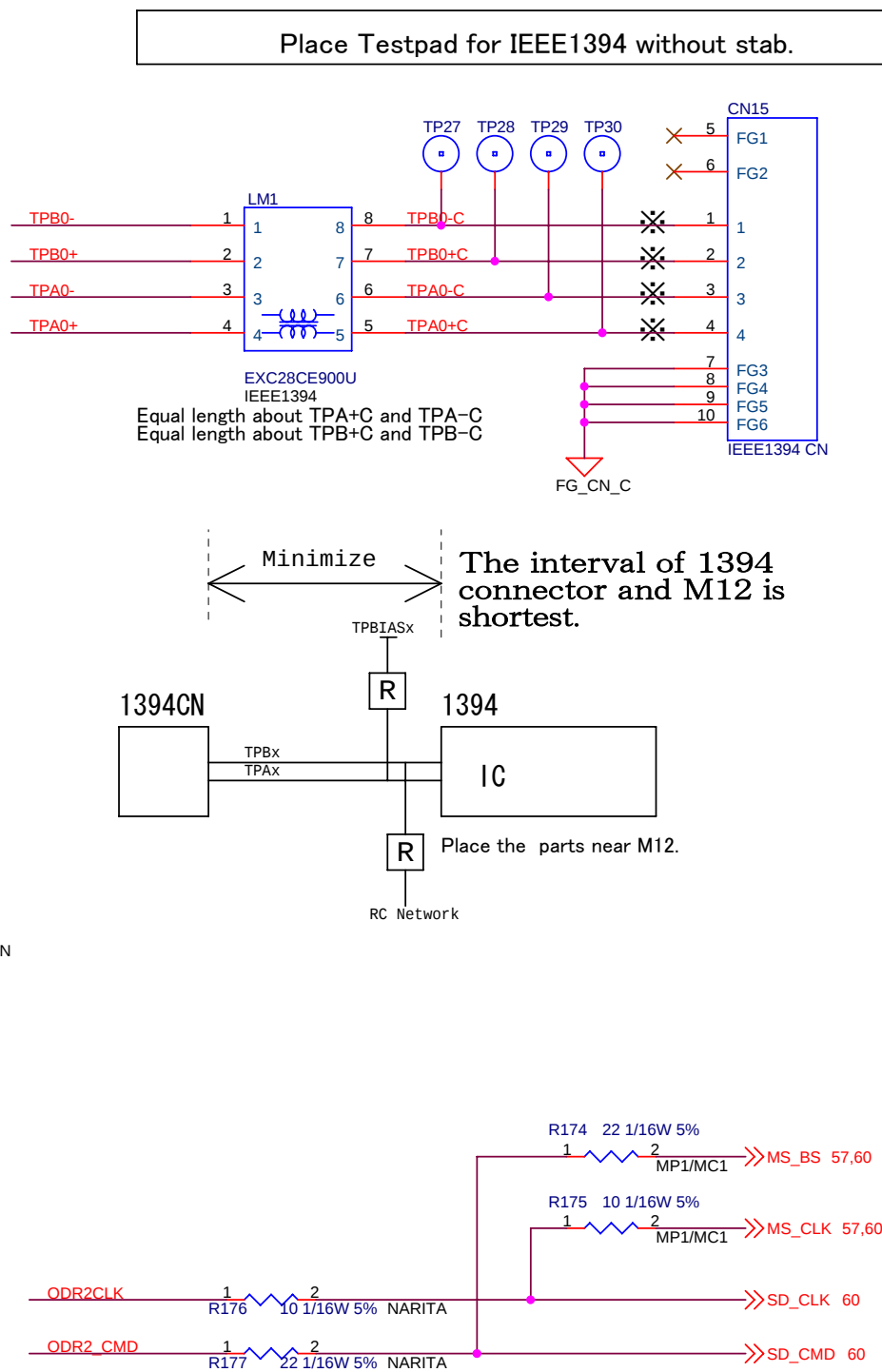
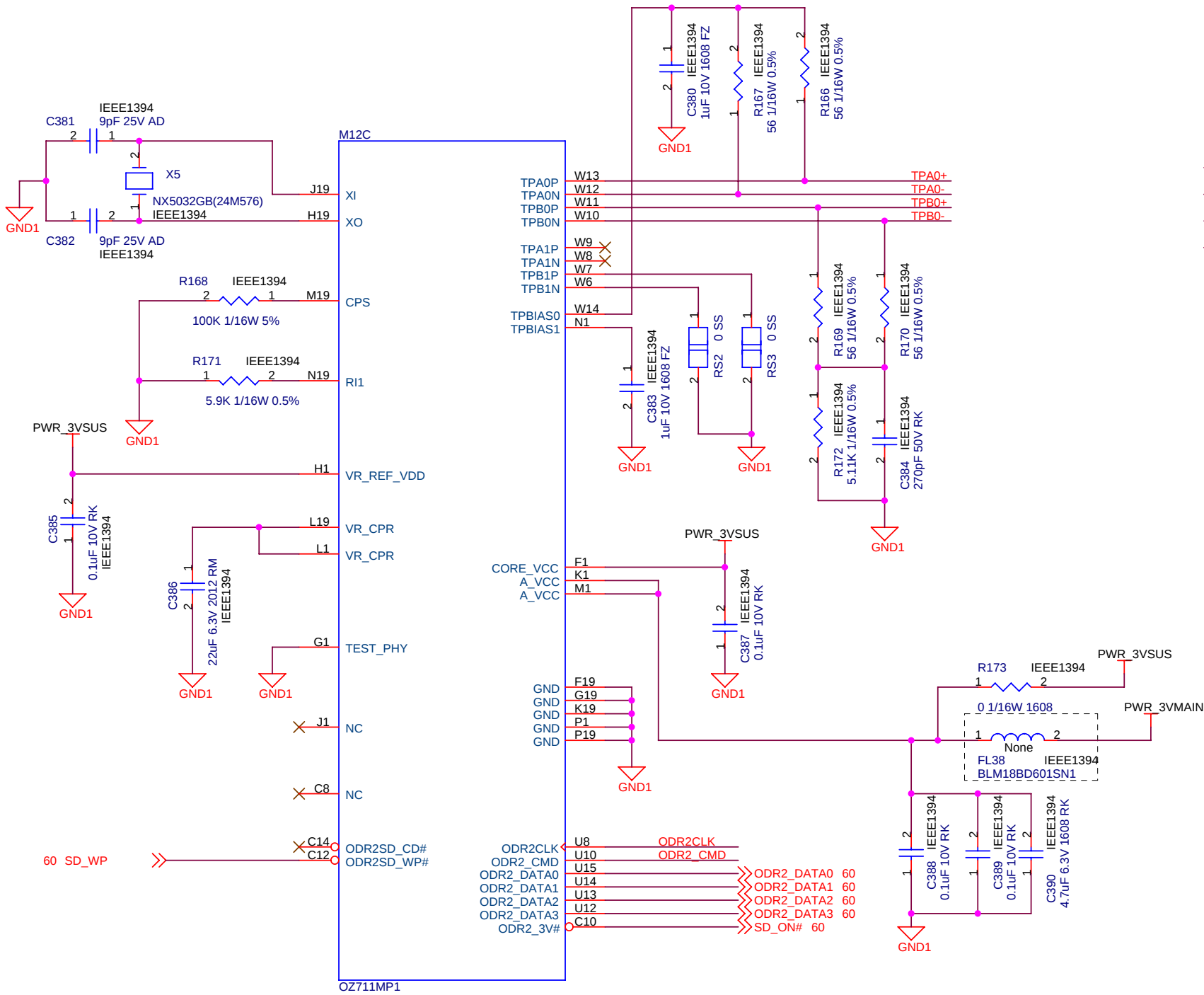
Place this clock dumping register near PCIC.



本抵抗はIC近傍に配置

JAA16はCardBus時に
クロック信号になるので
GND1にてガードをすること。

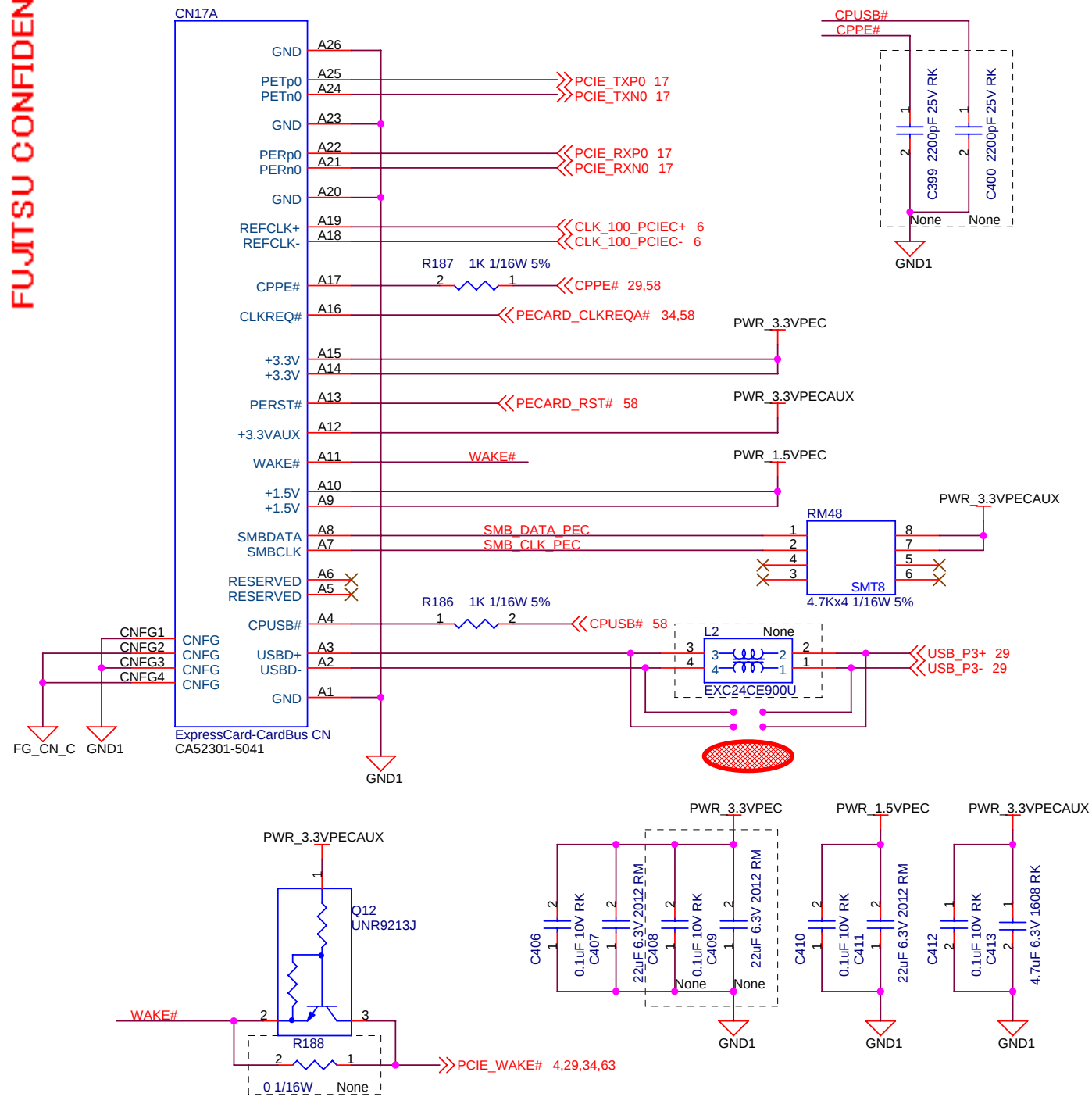
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									C1CP302570-X2	
									CAST	
Rev.	Date	Design	Check	Appr.	Description					
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD. Sheet 58 / 93	



IEEE1394 CN

									TITLE	
									VB313AA	
									DRAW. No.	
									CAST	
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD.		59 / 93

SLOT #1



05/11
部品変更
Q12 : DTC144EE (CA47001-0312) -->
DTC144EETL (CA471005016)

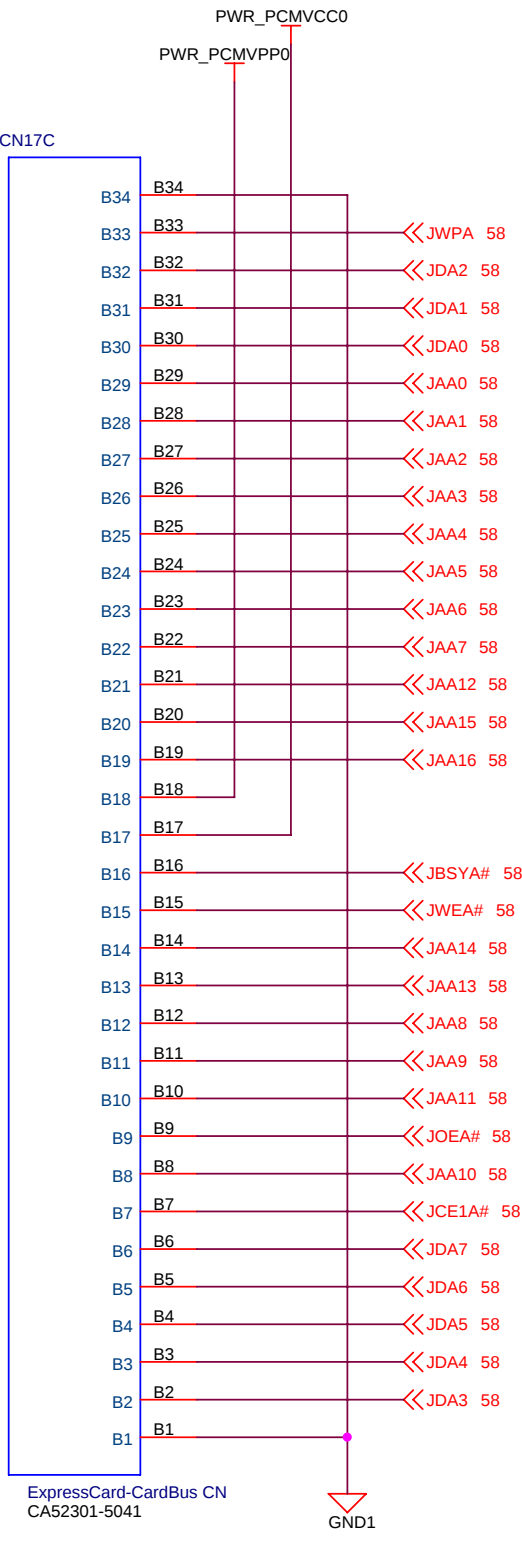
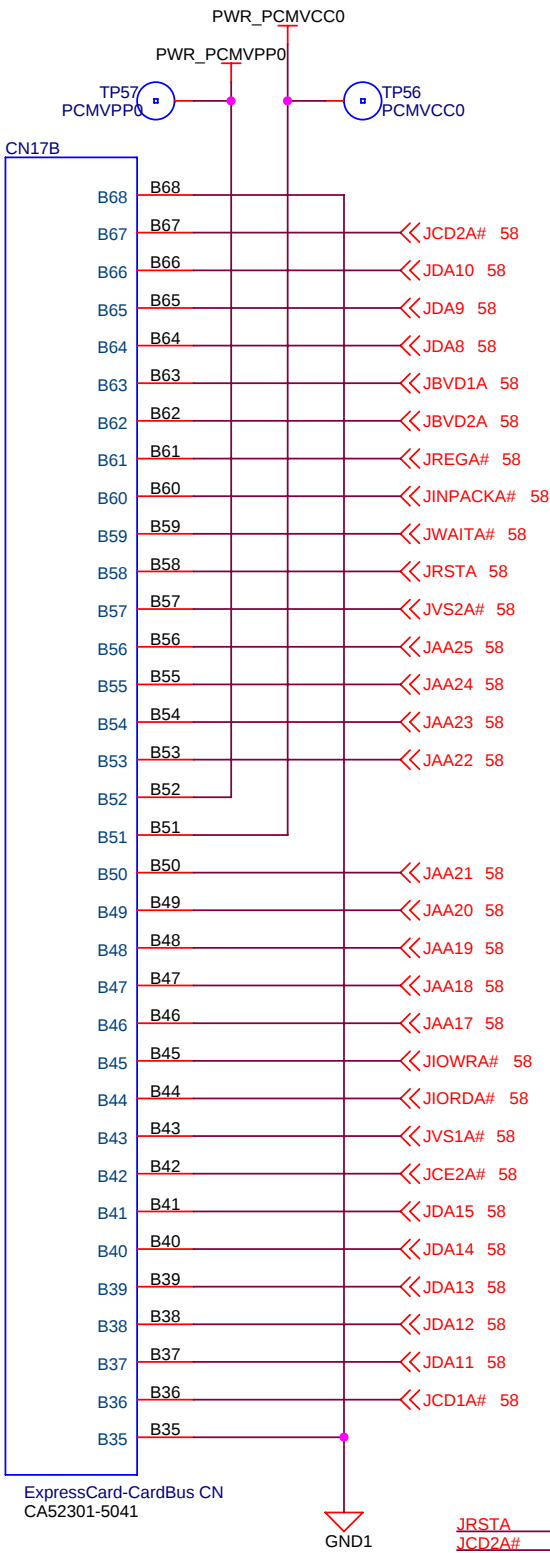
Fujitsu
Proprietary &
Confidential

FGはGND1に接続してください。

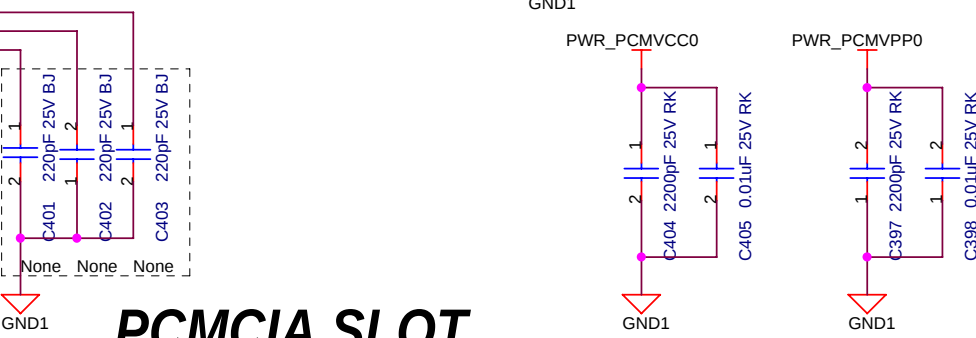
Express Card SLOT
PCMCIA SLOT

PCB

SLOT #0

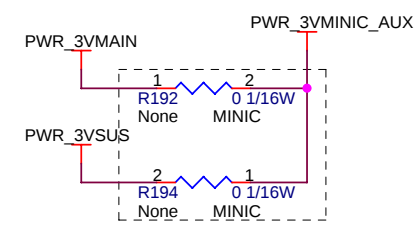
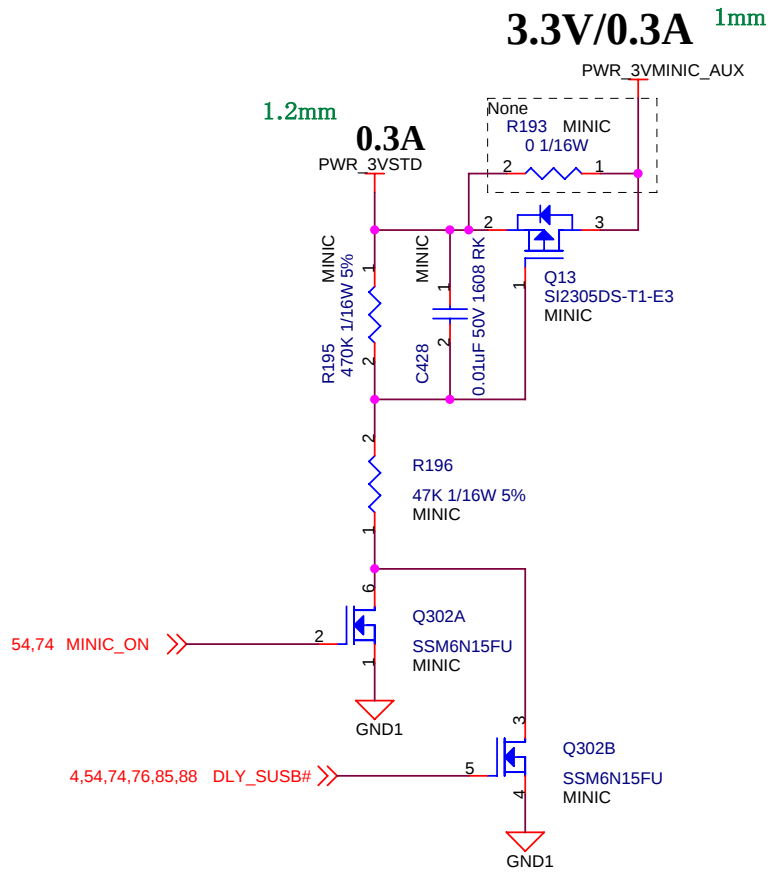
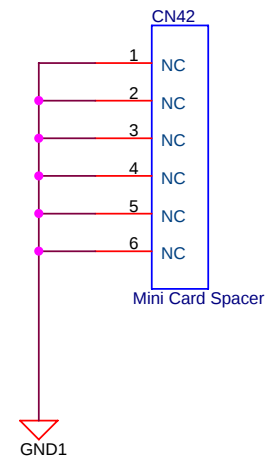
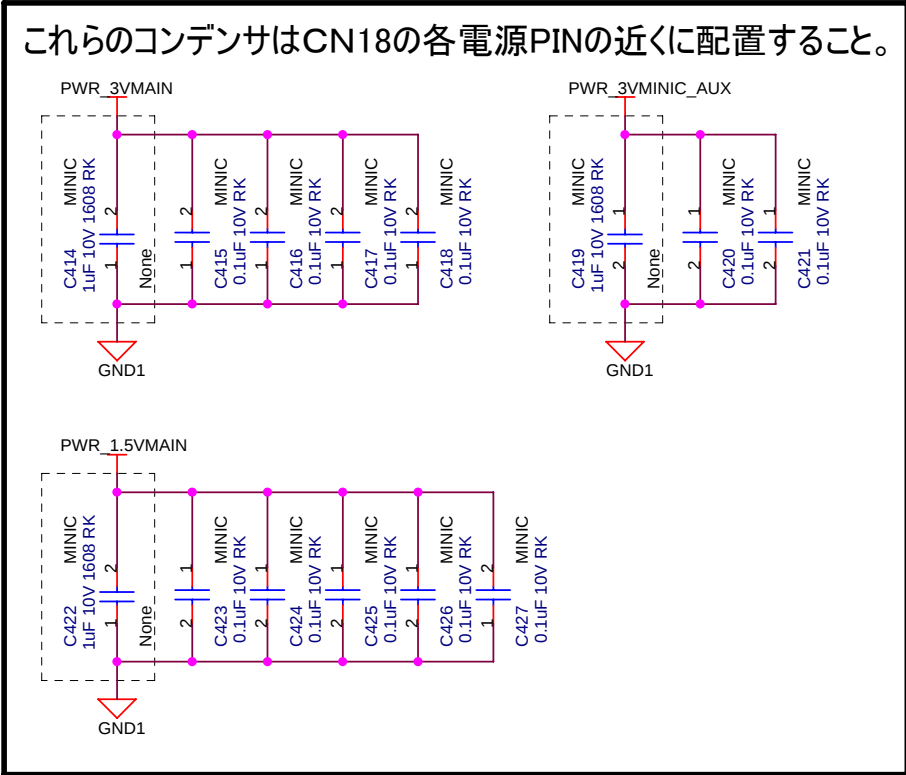
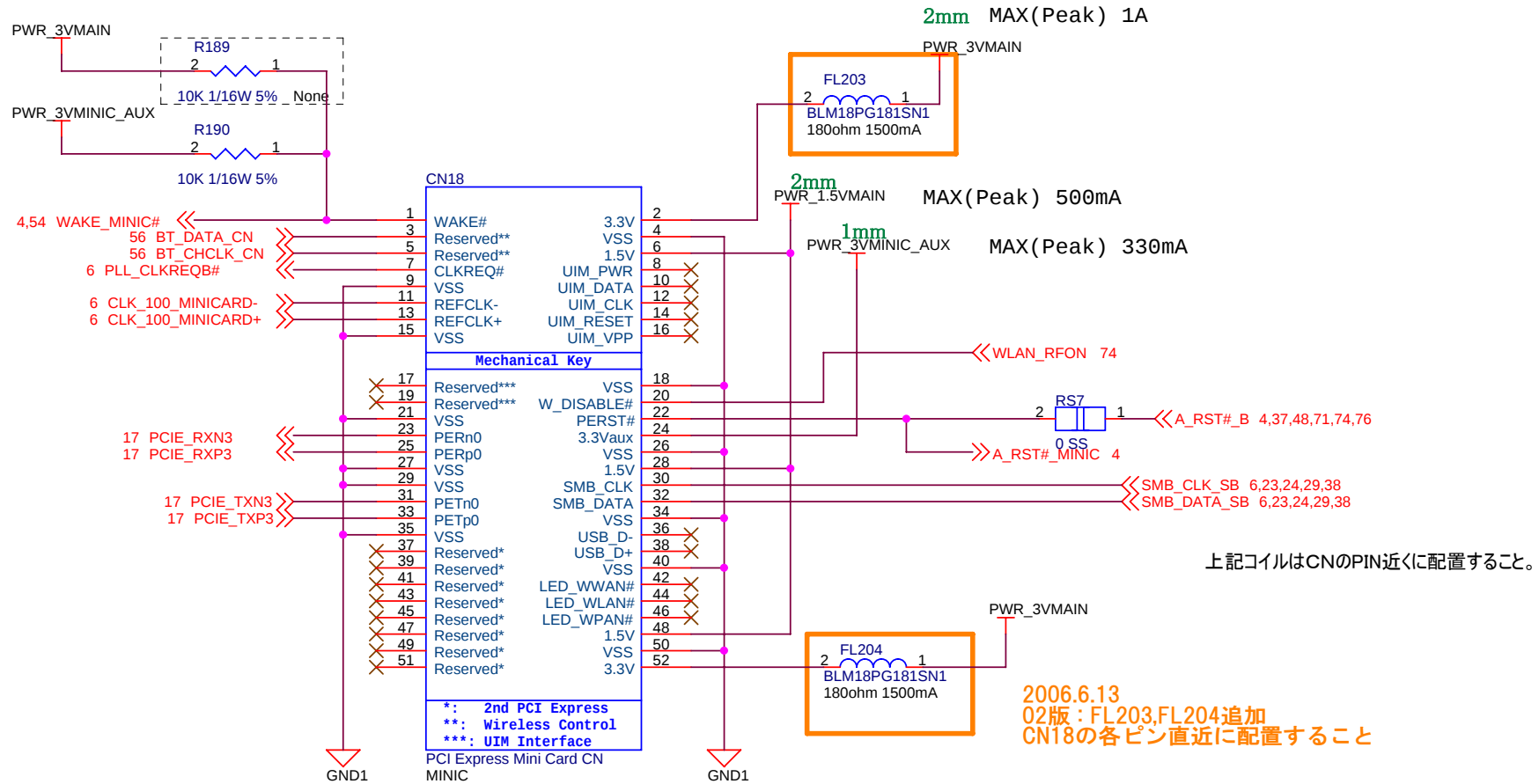


PCMCIA SLOT



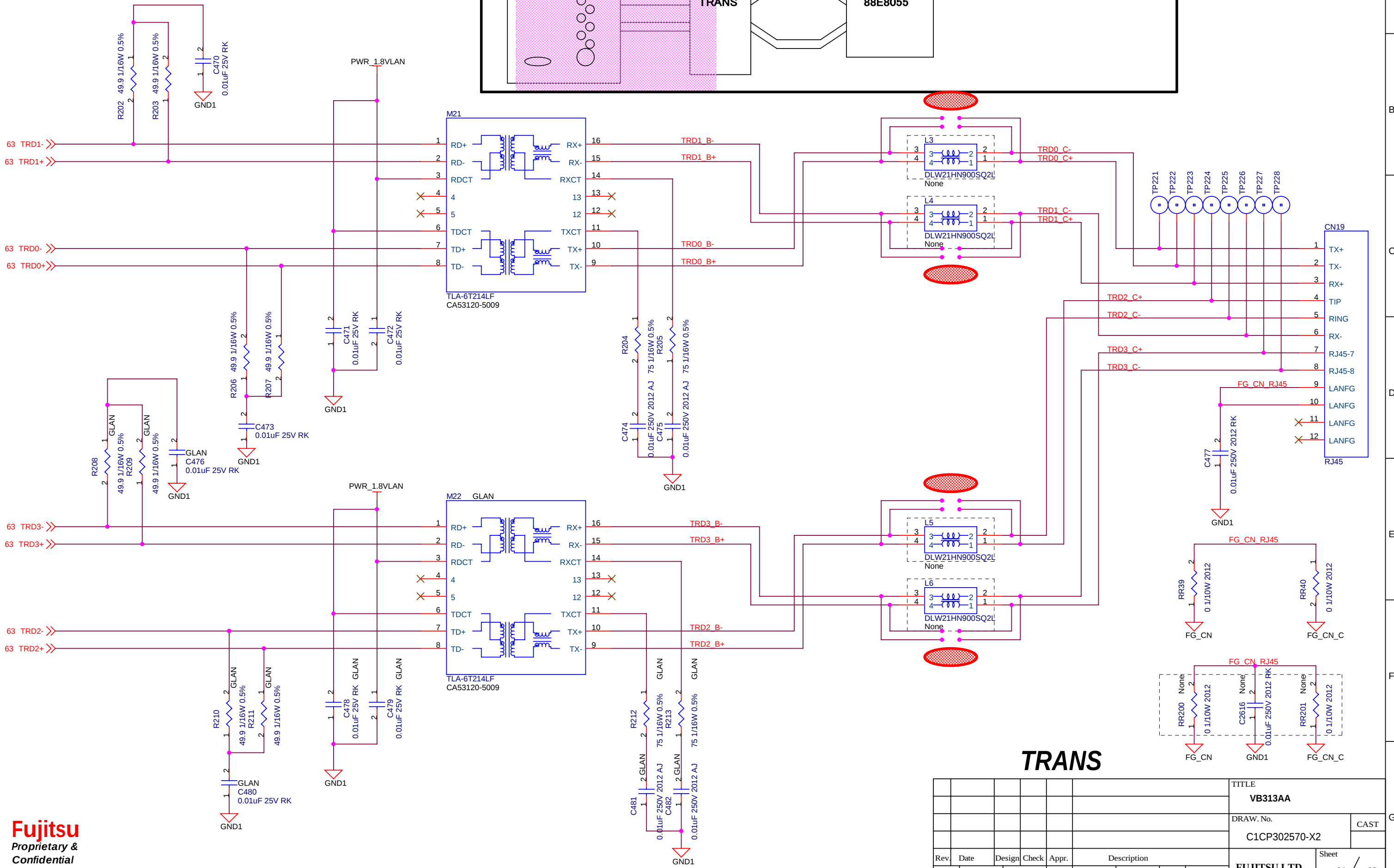
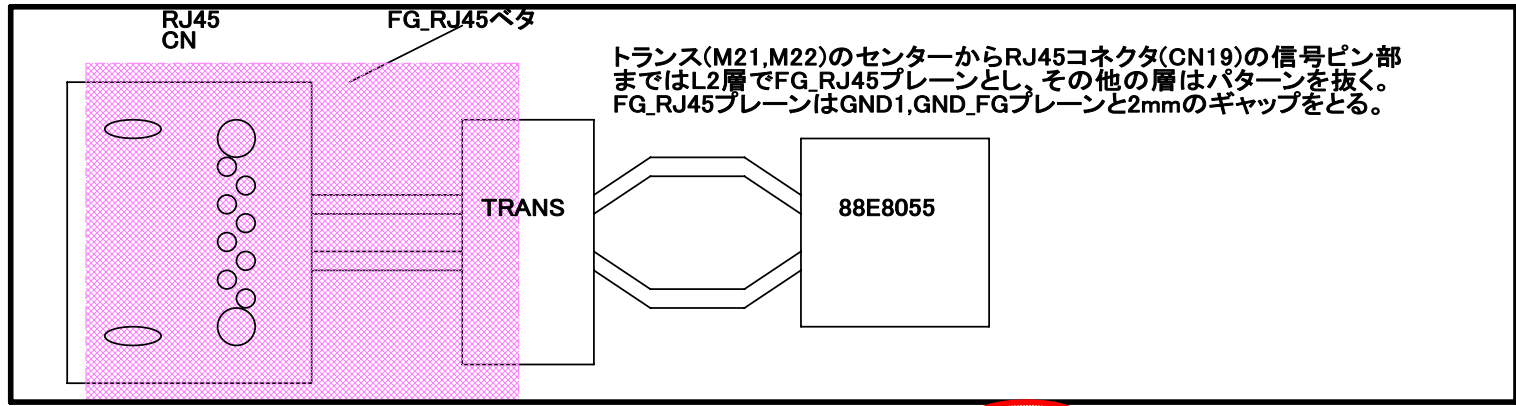
								TITLE	
								VB313AA	
								DRAW. No.	C1CP302570-X2
								CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet	61 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD.	

A・Bスロットとも JCE1x#, JCE2x#, JOEx#, JWEx#は、データベースとの平行配線とならないように配線すること。



MiniCard CN

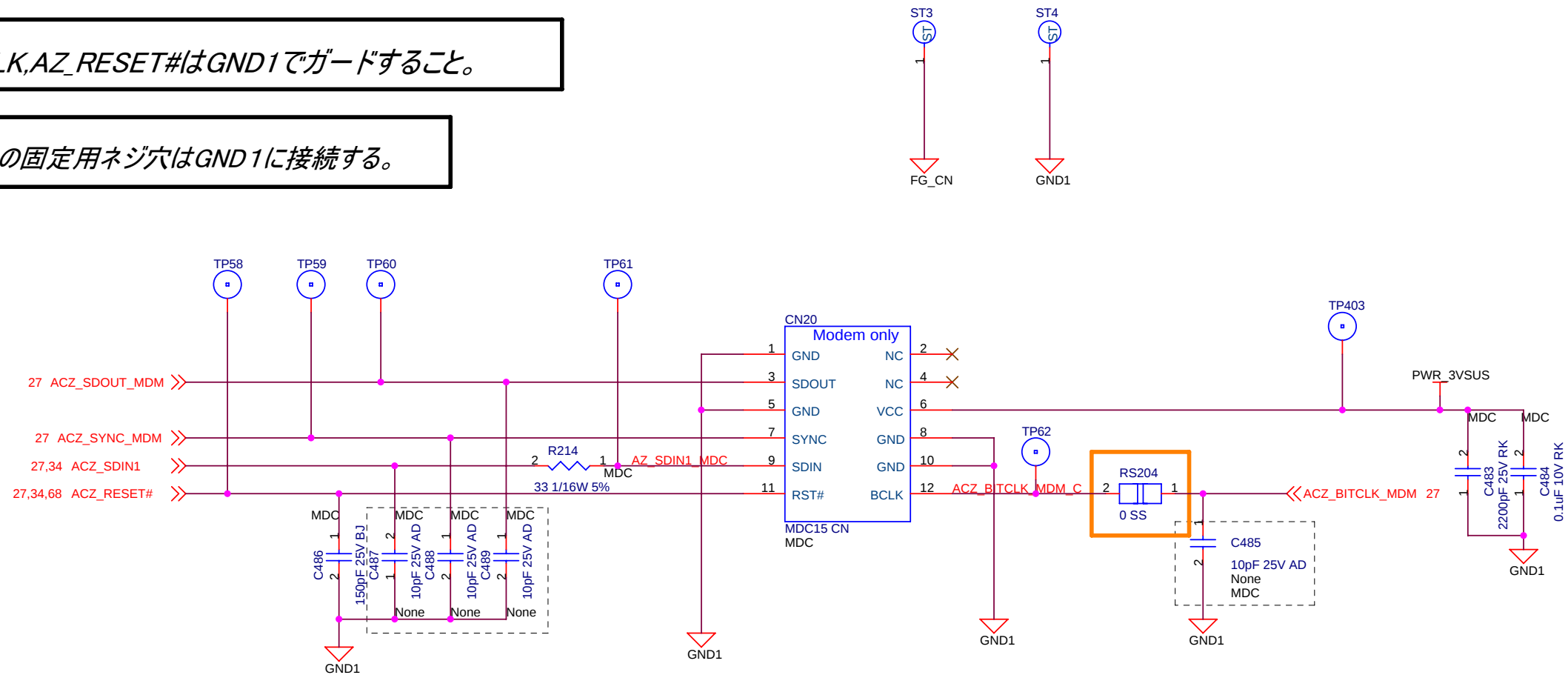
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						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		
Design	06/07/04	Mizukami	Check	Urita				
						Sheet		
						62 / 93		



TRANS

AZ_BITCLK,AZ_RESET#はGND1でガードすること。

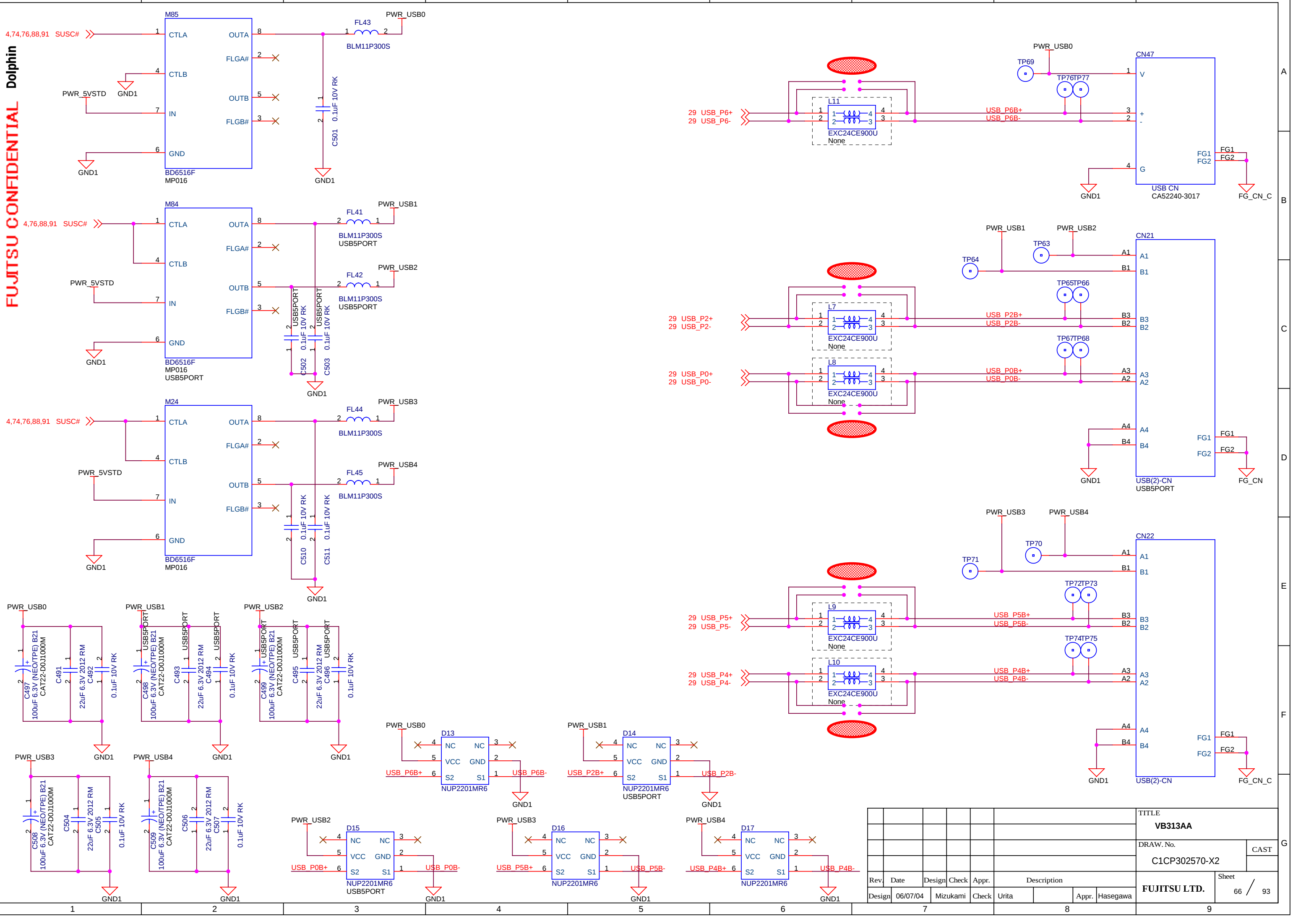
モジュールの固定用ネジ穴はGND1に接続する。



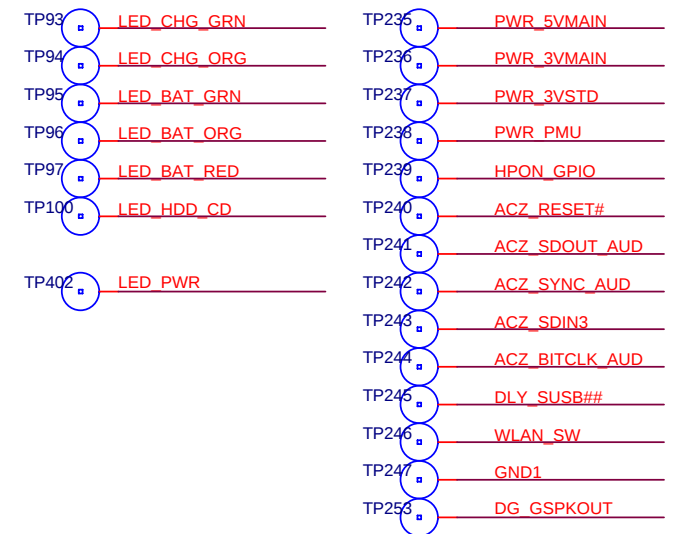
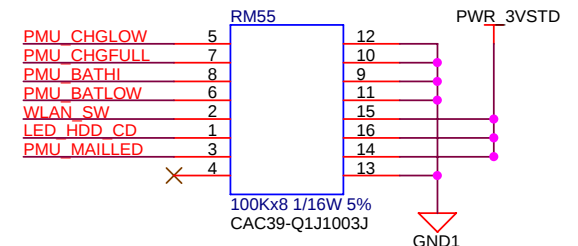
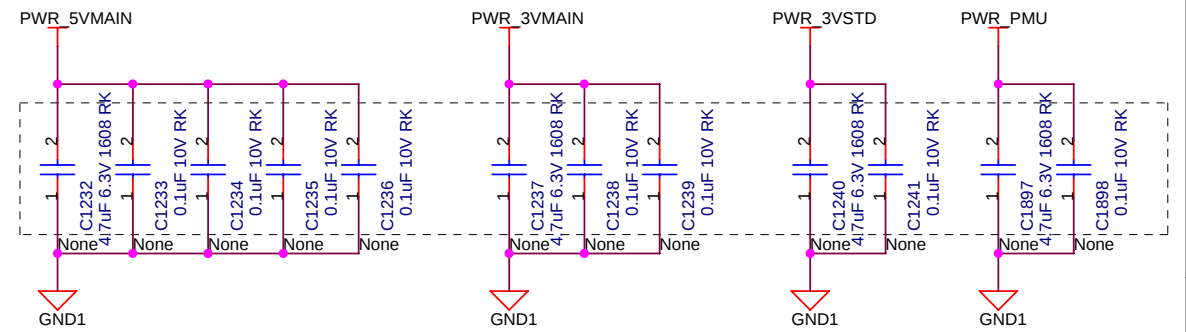
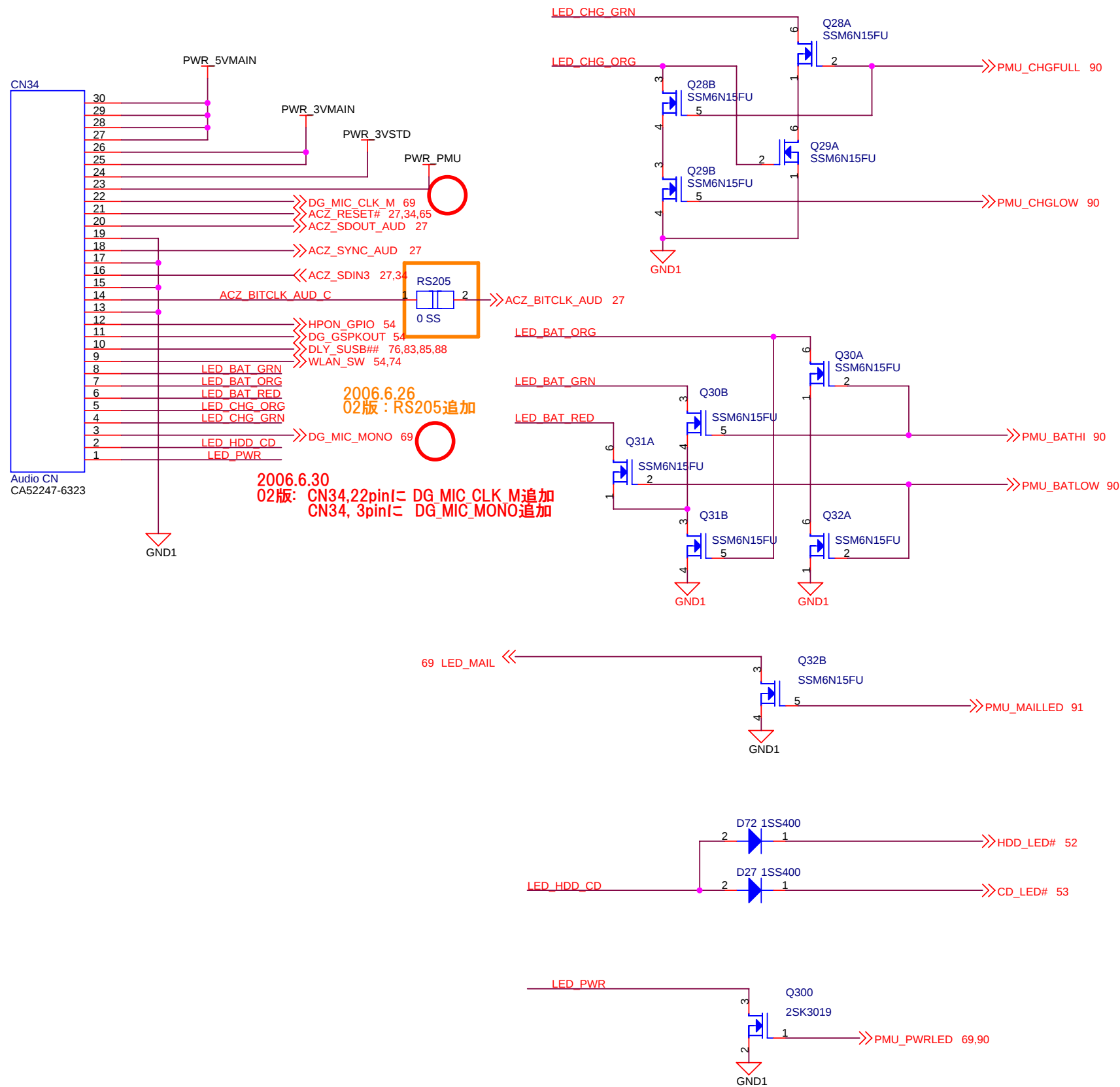
2006.6.26
02版：RS204追加

MDC Modem

						TITLE		
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						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	65 / 93

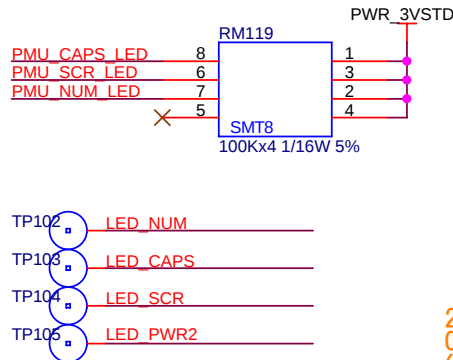
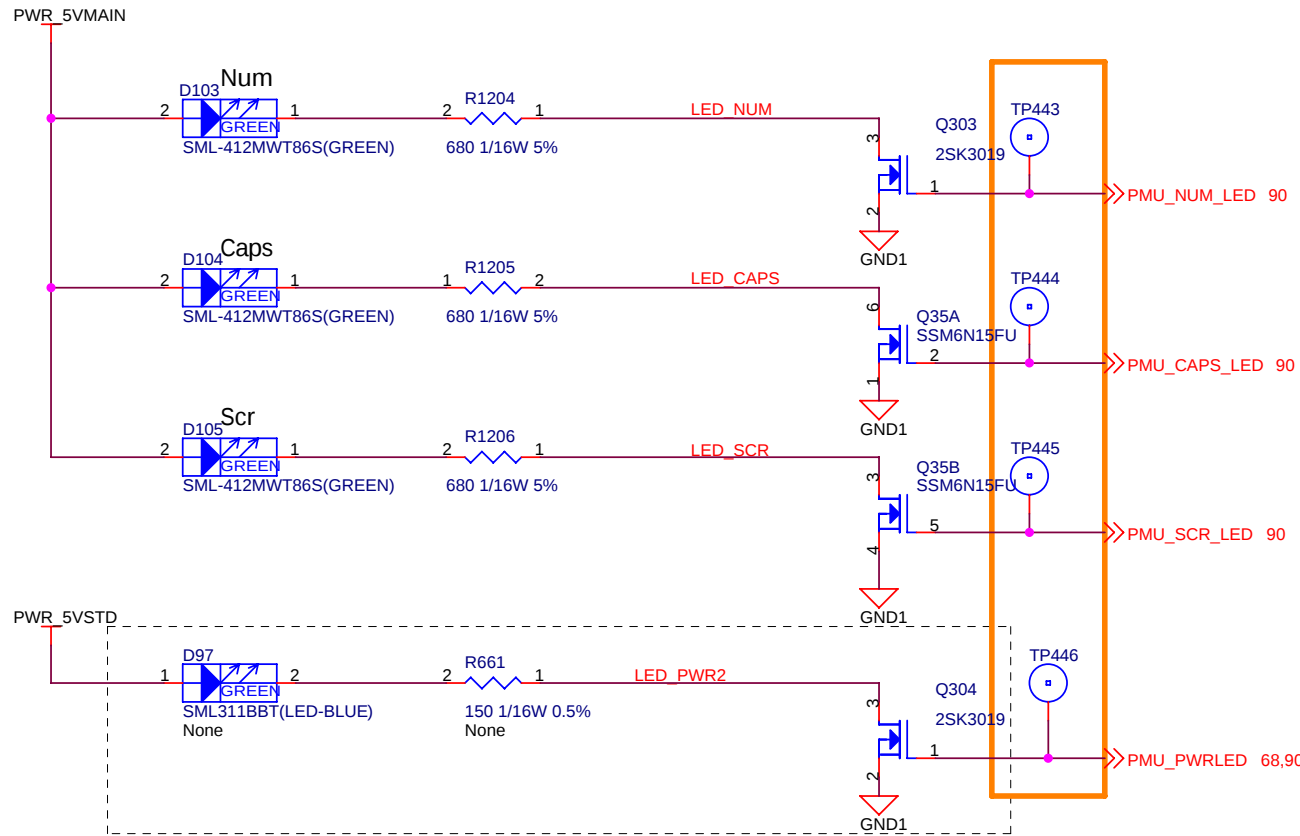


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						DRAW. No.		CAST
						C1CP302570-X2		
						FUJITSU LTD.		Sheet
Rev.	Date	Design	Check	Appr.	Description	66 / 93		
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa			



Audio/Statu CN

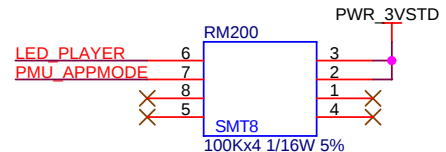
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						VB313AA				
						DRAW. No.			CAST	
						C1CP302570-X2				
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	68 / 93		



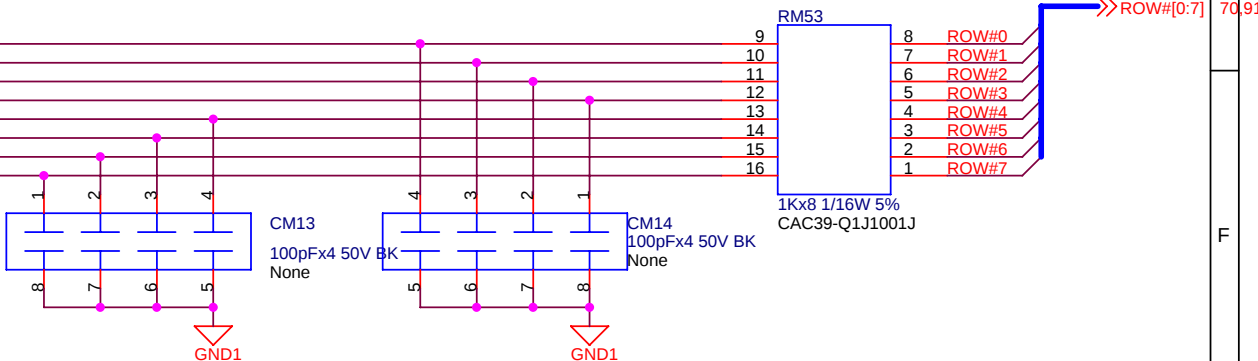
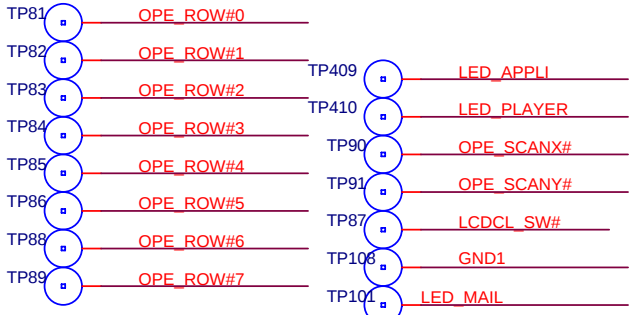
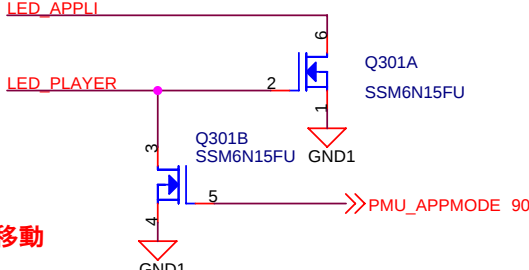
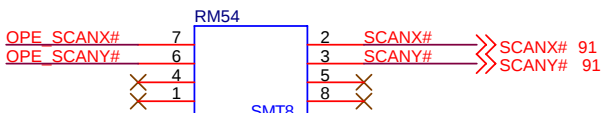
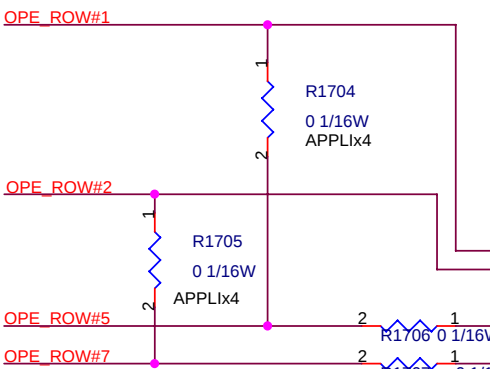
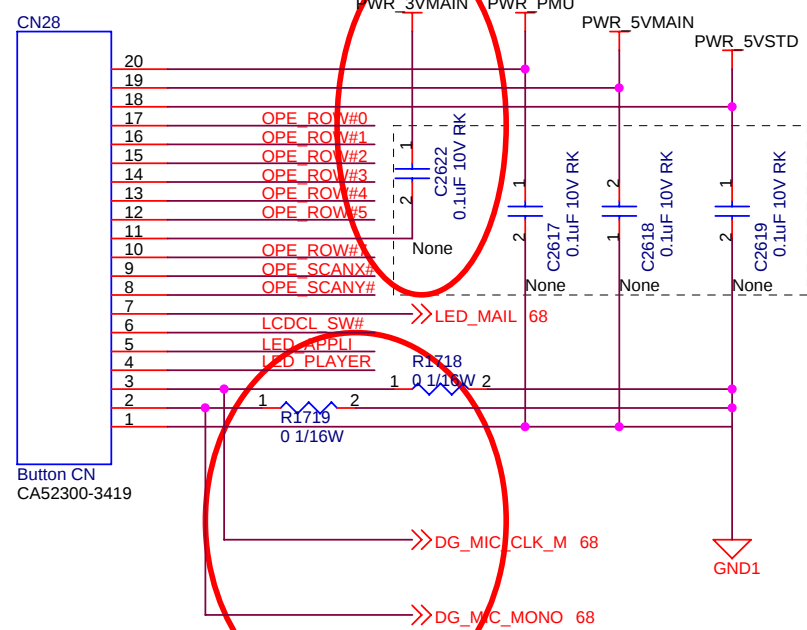
2006.6.26
02版: 電源ボタンにTP追加
(Fennecと配置の共通化をお願いします)

2006.6.26
02版: 電源ボタン変更
CA49001-5370 --> CA49001-5119

2006.6.26
02版:
LEDにTP追加。TP443,TP444,TP445,TP446
(Fennecと配置の共通化をお願いします)



- ROW#0 SW_Mode
- ROW#1 SW_Appli-A
- ROW#2 SW_Appli-B
- ROW#3 SW_Internet
- ROW#4 SW_Mail
- ROW#5 SW_Vol_Down
- ROW#6 Unused
- ROW#7 SW_Vol_up

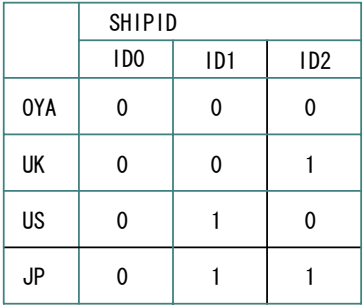


[Button CN]

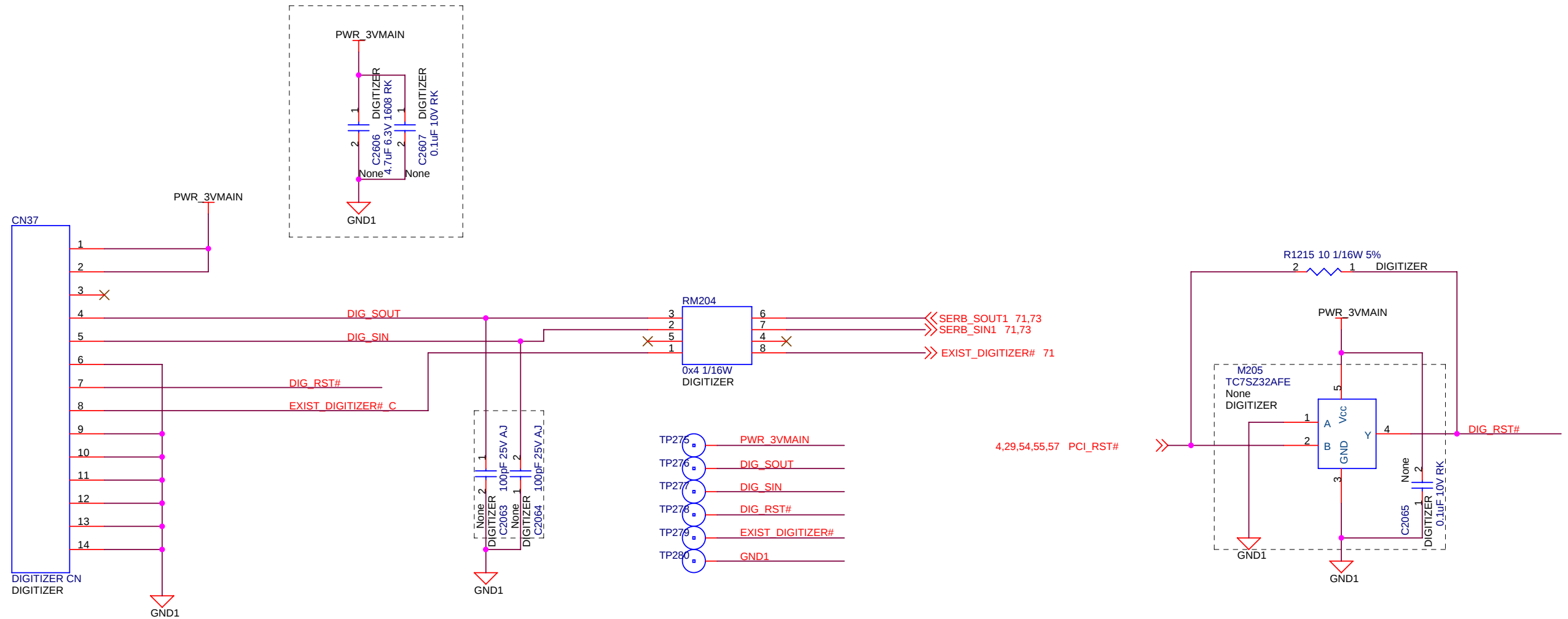
2006.6.30
02版: R1718-1721,C2622追加
2006.7.04
R1720,R1721をMainボードからAudioボードへ移動

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
						FUJITSU LTD.		Sheet
						69 / 93		
Rev.	Date	Design	Check	Appr.	Description			
Design	06/07/04	Mizukami	Check	Urita				

Fujitsu
Proprietary & Confidential

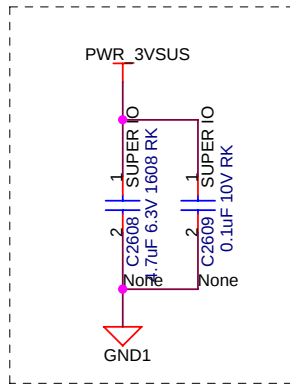
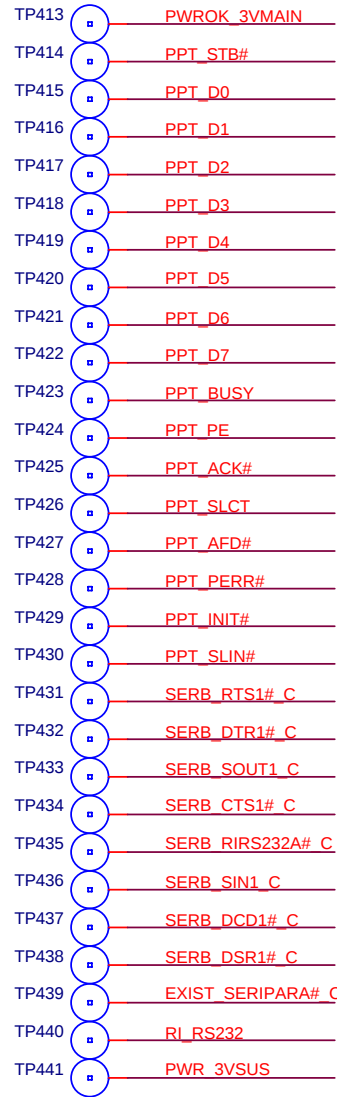


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									DRAW. No.	C
									C1CP302570-X2	AST
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet 70 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa			



DIGITIZER CN

									TITLE VB313AA		G	
									DRAW. No.			CAST
									C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.		Sheet 72 / 93	
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa				



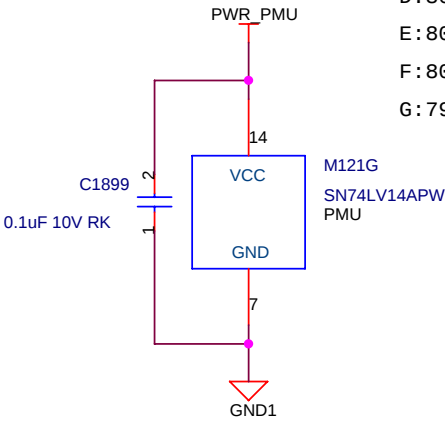
本ページの部品は、I/O-CNの近くに配置すること

PARALLEL/SERIAL CN

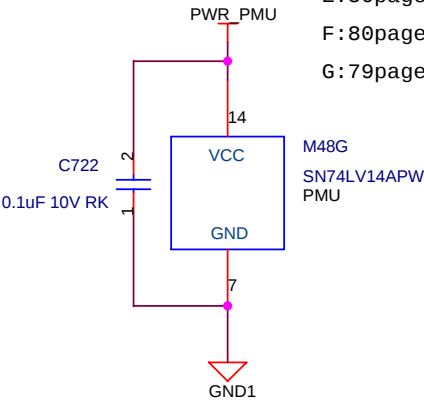
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Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		73 / 93

PWR_3VSUS to BENN_SUSOK
Default 50ms

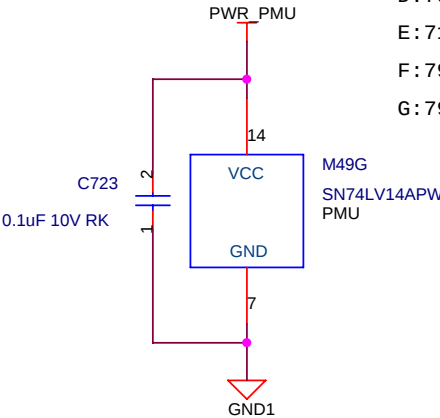
PWR_3VMAIN to BENN_MAINOK
Default 170ms



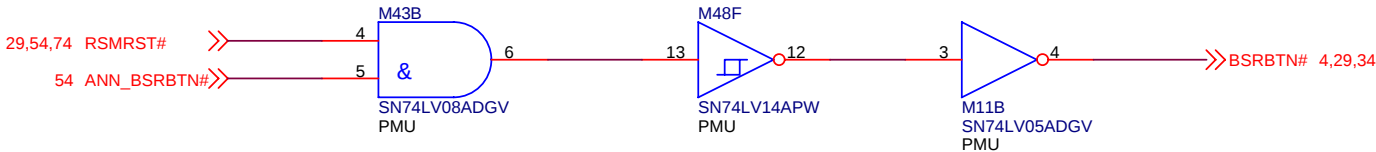
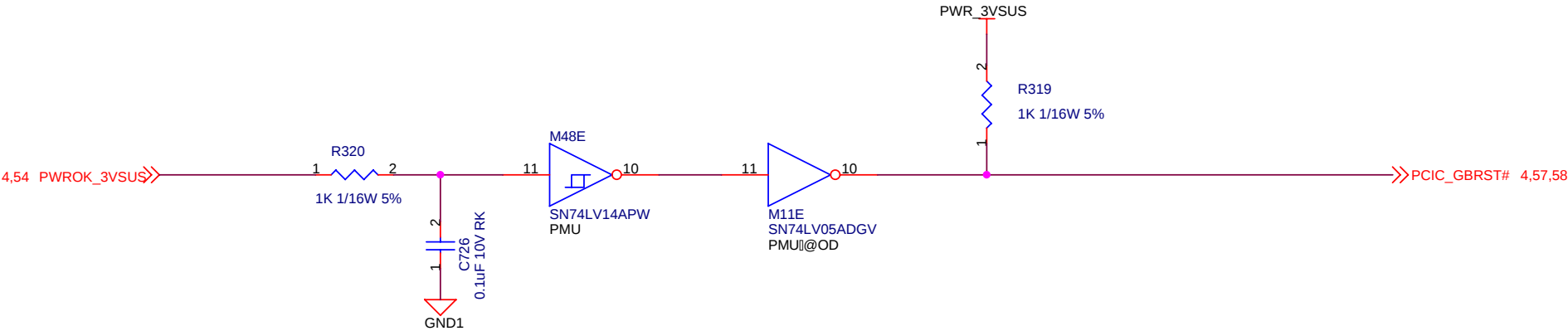
A: 80page
B: 80page
C: 80page
D: 80page
E: 80page
F: 80page
G: 79page



A: 80page
B: 80page
C: 80page
D: 80page
E: 80page
F: 80page
G: 79page



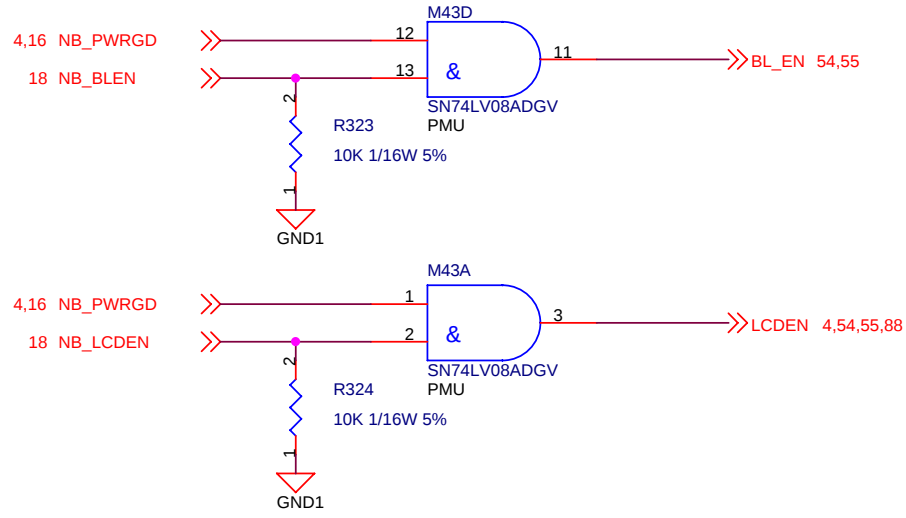
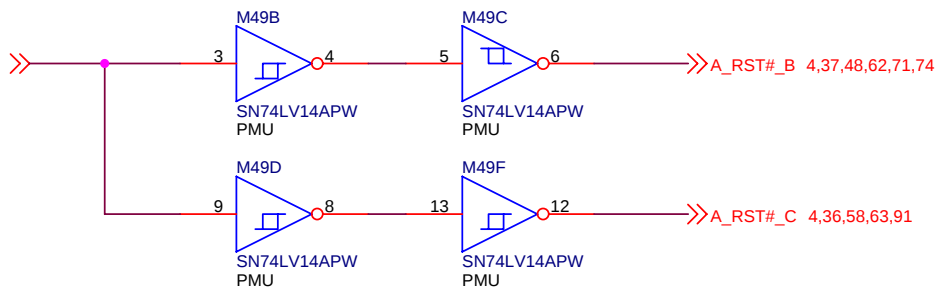
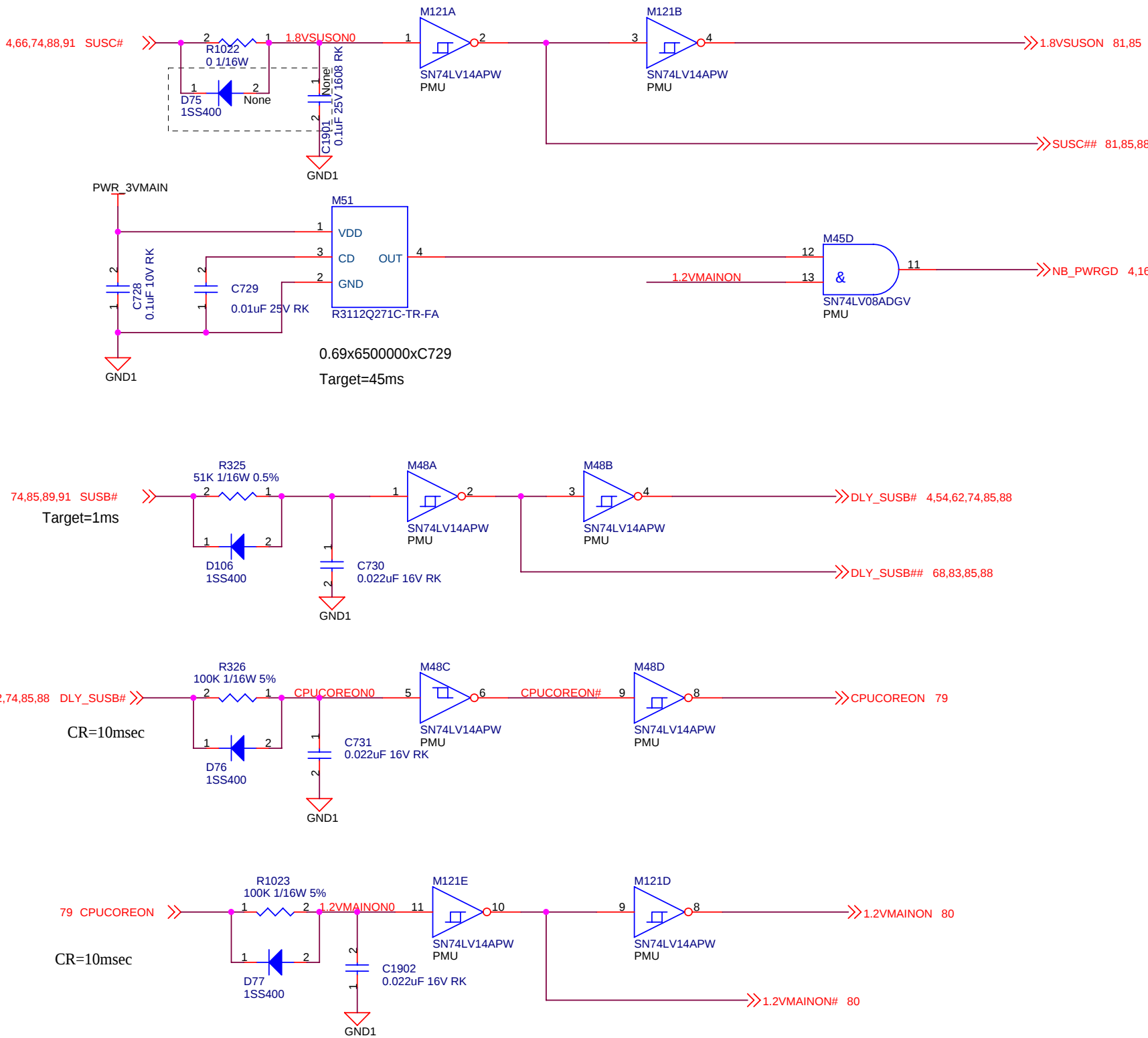
A: 80page
B: 80page
C: 80page
D: 79page
E: 71page
F: 79page
G: 79page



遅延ターゲット
BD5327G:
 $T_{plh}(s) = 0.69(TYP) \times 9(M\Omega) \times CT(F)$

RESET IC

						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD. 75 / 93



SEQUENCE

									TITLE	
									VB313AA	
									DRAW. No.	
									C1CP302570-X2	
									CAST	
Rev.	Date	Design	Check	Appr.	Description					
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD.	
									Sheet 76 / 93	

Falcon Power Supply

Caution

Features

- 1/ Voltage Regulator for AMD K8 Rev.F Processor
- 2/ ATI RS480M Chipset
- 3/ DDR2 Memory
- 4/ Internal VGA (PowerPlay is not supported)
- 5/ Normal Speed Charger
- 6/ 19V AC Adaptor
- 7/ A circuit reducing a rush current from AC adaptor
- 8/ Internal Battery with 4 or 3 Seirial cells and Digital Interface

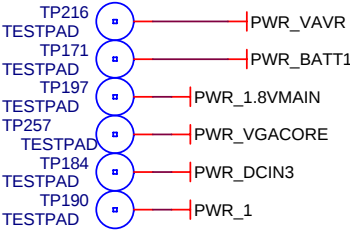
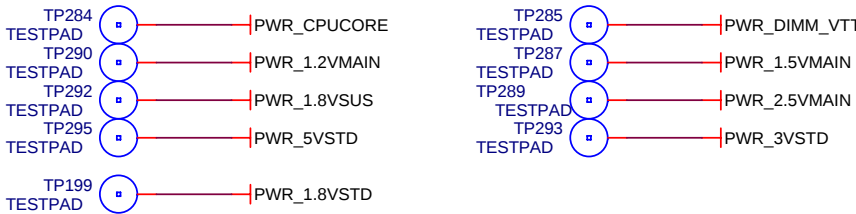
Voltage Regulator Spec.

DDC	CPUCore	TBD	35A	typ/peak
	1.2VMain	1.200V +/-5% (1.140V-1.260V)	6A	typ / 8Apeak
	1.8VSus	1.800V +/-5% (1.710V-1.890V)	6A	typ / 8Apeak
	3VStd	3.300V +/-5% (3.135V-3.465V)	6A	typ / 8Apeak
	5VStd	5.000V +/-4% (4.800V-5.200V)	6A	typ / 8Apeak
Charger	CV 3-serial	12.60V +/-1.2% (12.45V-12.75V)	CC 1.33A	
	CV 4-serial	16.80V +/-1.2% (16.60V-17.00V)	CC 1.33A	
LDO	DimmVtt	0.900V +/-100mV (0.800-1.000V)	+/-0.25A typ / +1Apeak	
	1.5VMain	1.500V +/-5% (1.425V-1.575V)	1A	
	1.8VStd	1.800V +/-5% (1.710V-1.890V)	0.3A	
	2.5VMain	2.500V +/-5% (2.375V-2.625V)	40mA	
	VAVR	3.300V +/-2% (3.234V-3.366V)	30mA	

Power Contents

Contents		Page#	Contents		Page#
DDC	TopPage	82	Node	DCIn,Battery	91
	Delivery	83		Switch1	92
				Switch2	93
	CPUCore	84	PMU	LUNA1 (PMU part)	94
	(reserved)	85		LUNA2 (KBC part)	95
LDO	1.05V/1.8V	86		Etc0 (Common)	96
	3.3V/5V	87		Etc1 (Battery1)	97
	(reserved)	88			
	Charger	89			
		90			

TestPad (for SFJ)

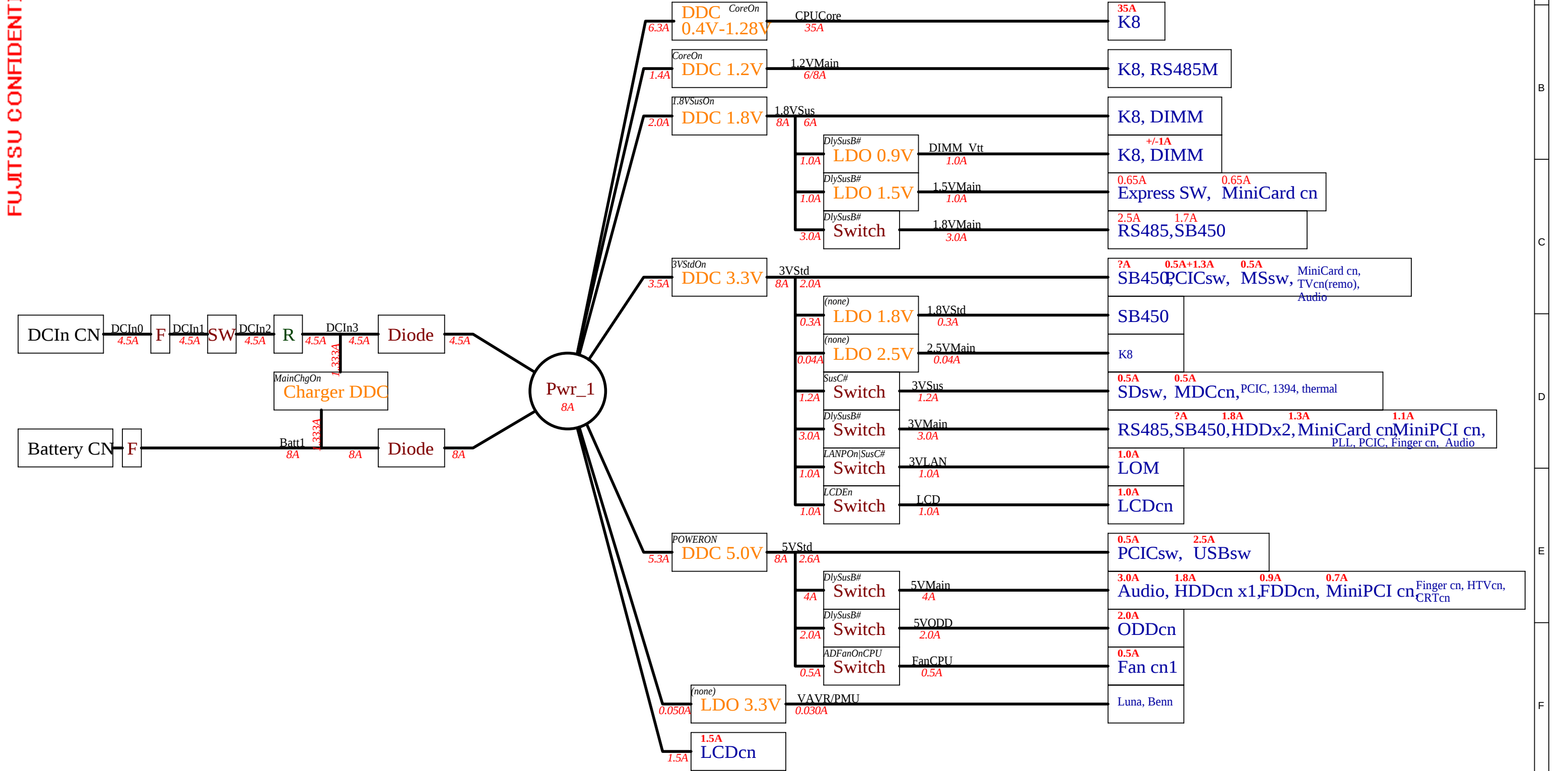


						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet 77 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

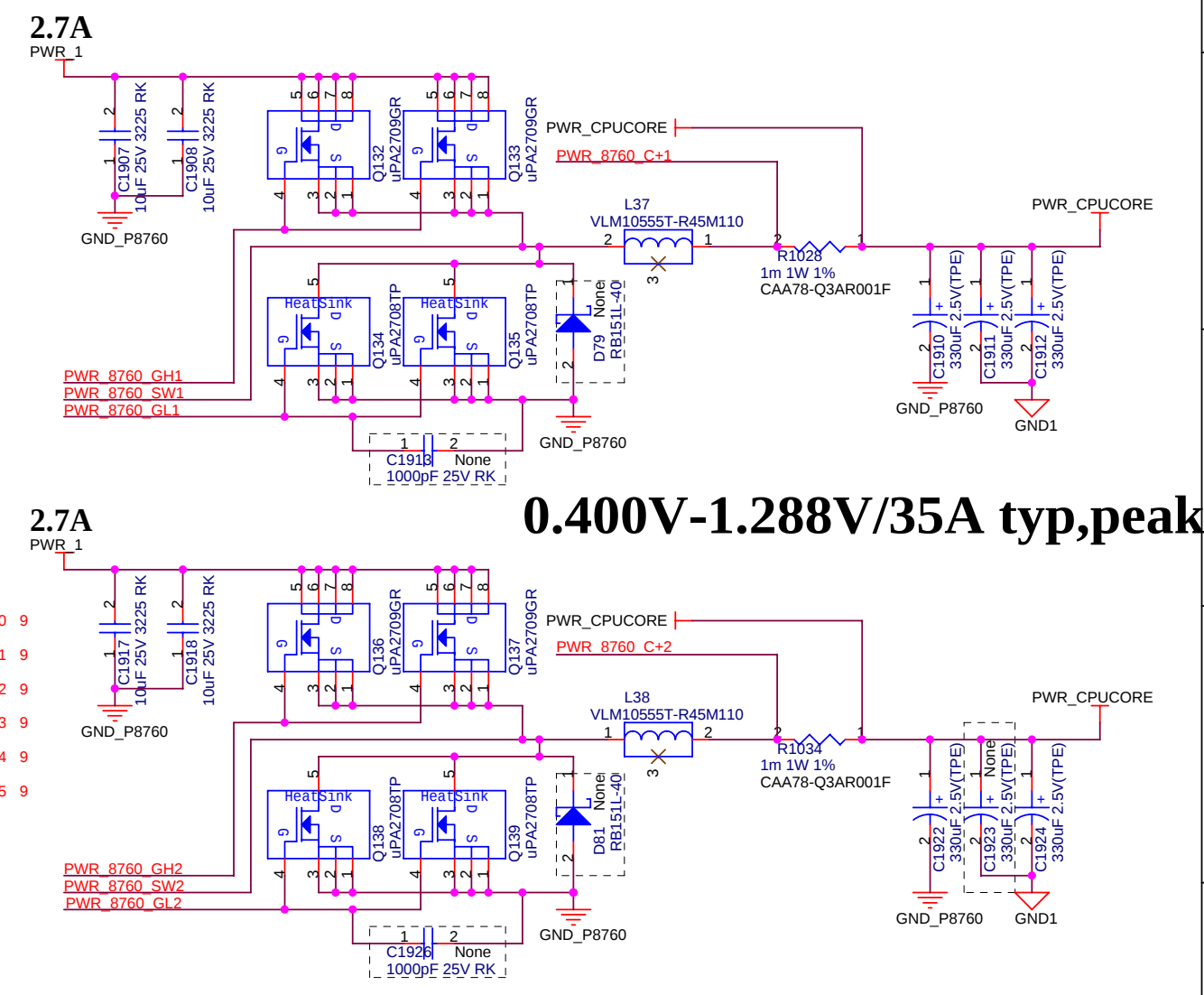
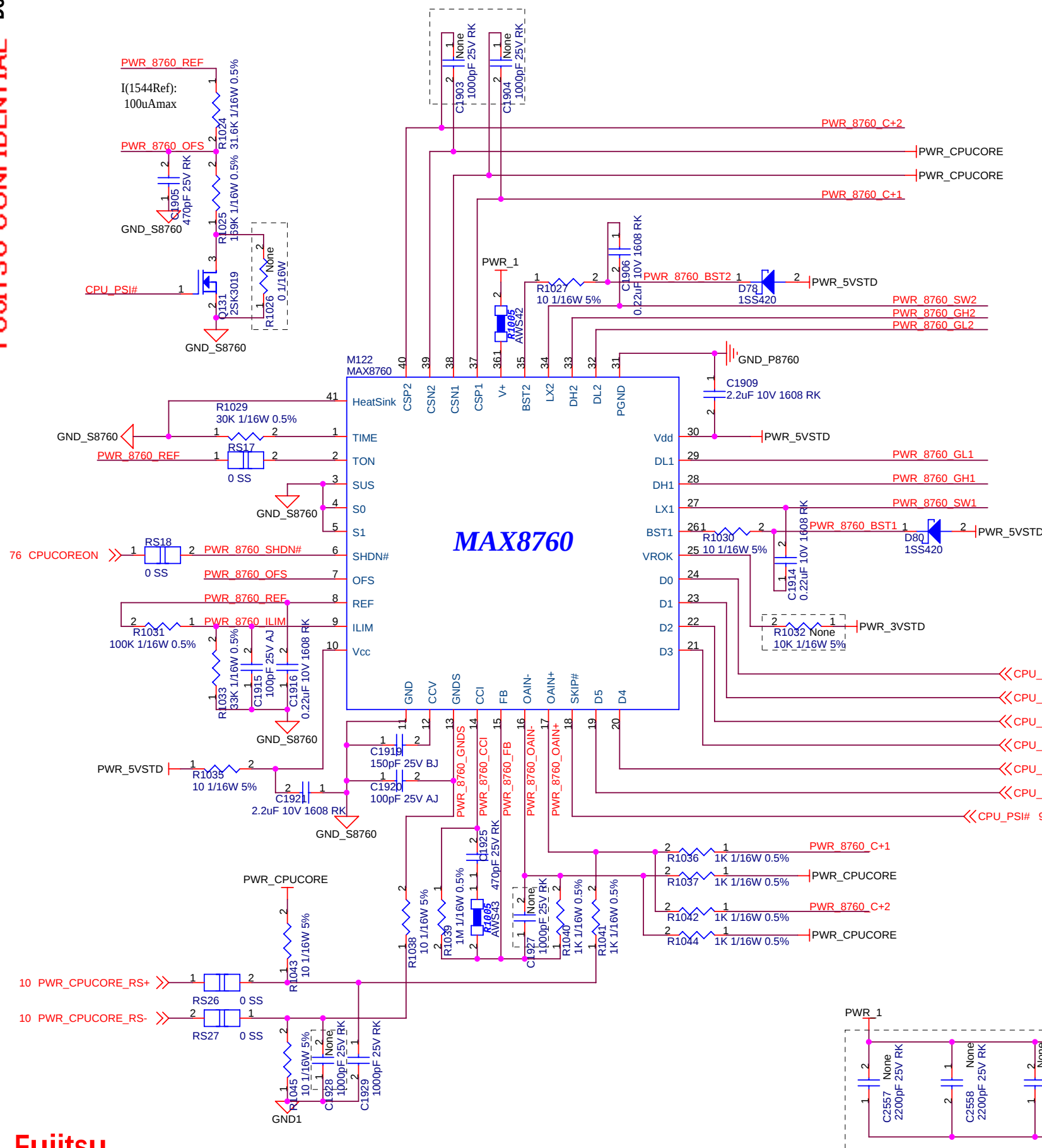
Dolphin

Power Delivery

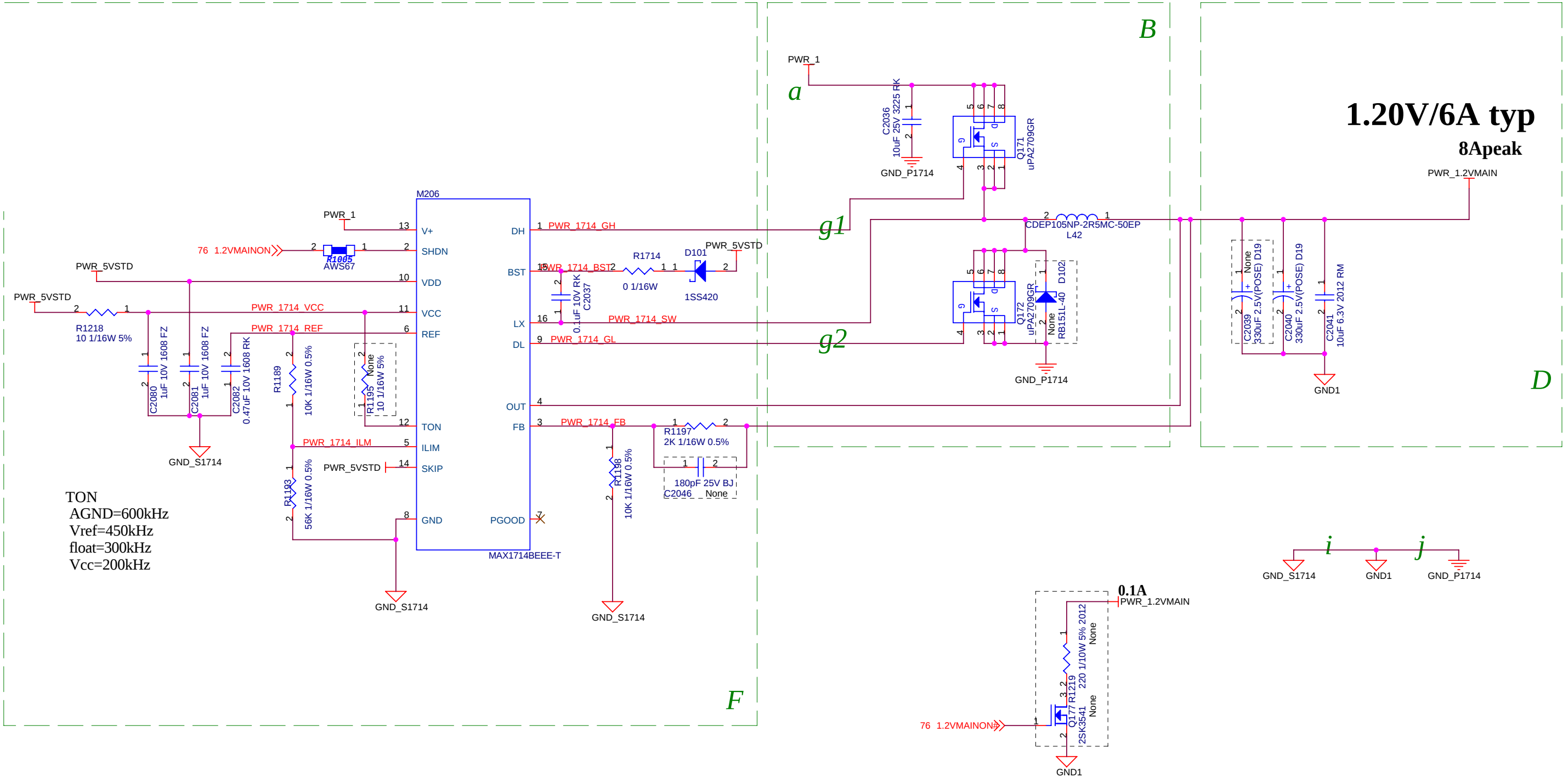
FUJITSU CONFIDENTIAL



						TITLE		
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						DRAW. No.		CAST
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Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	78 / 93

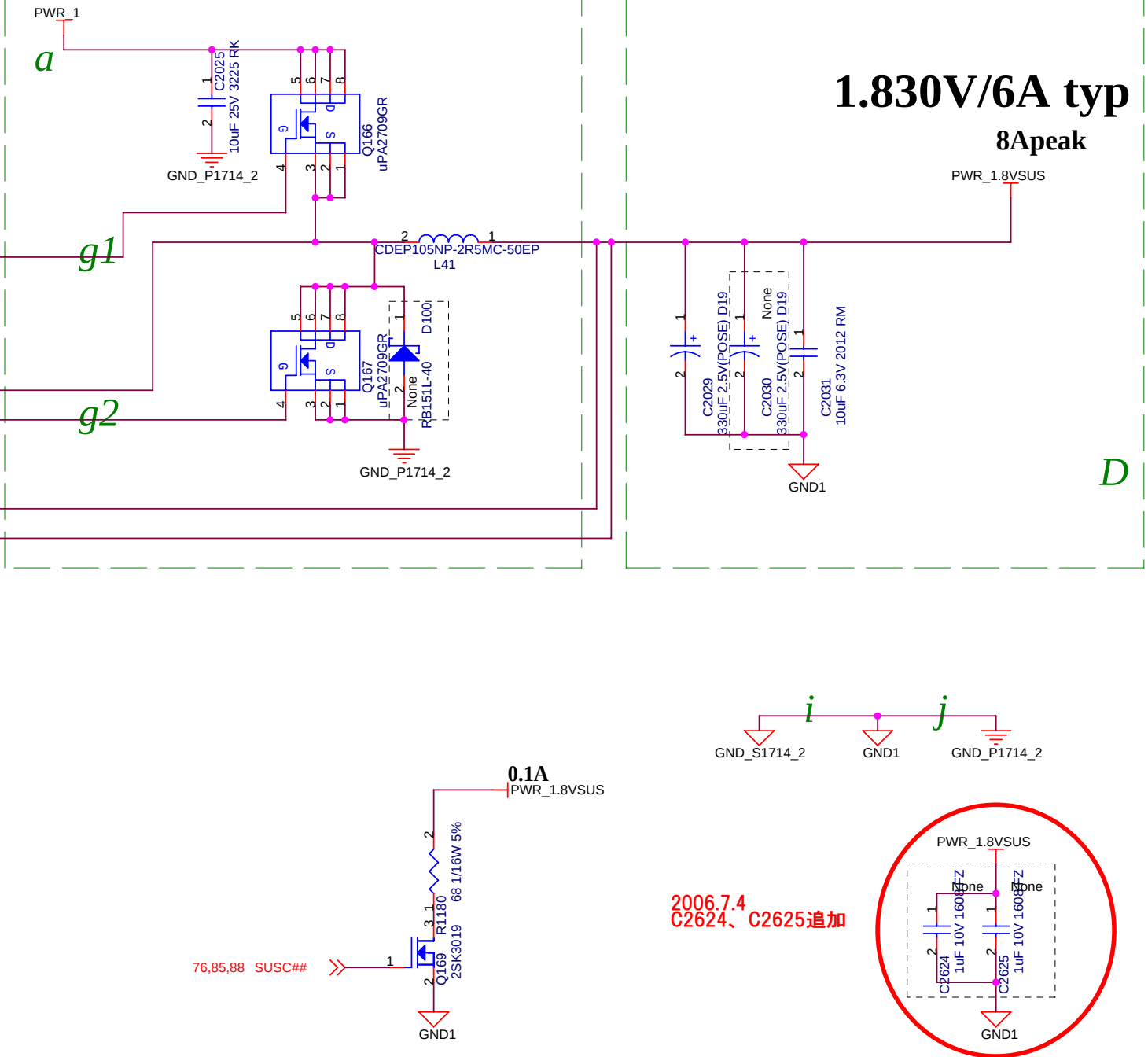
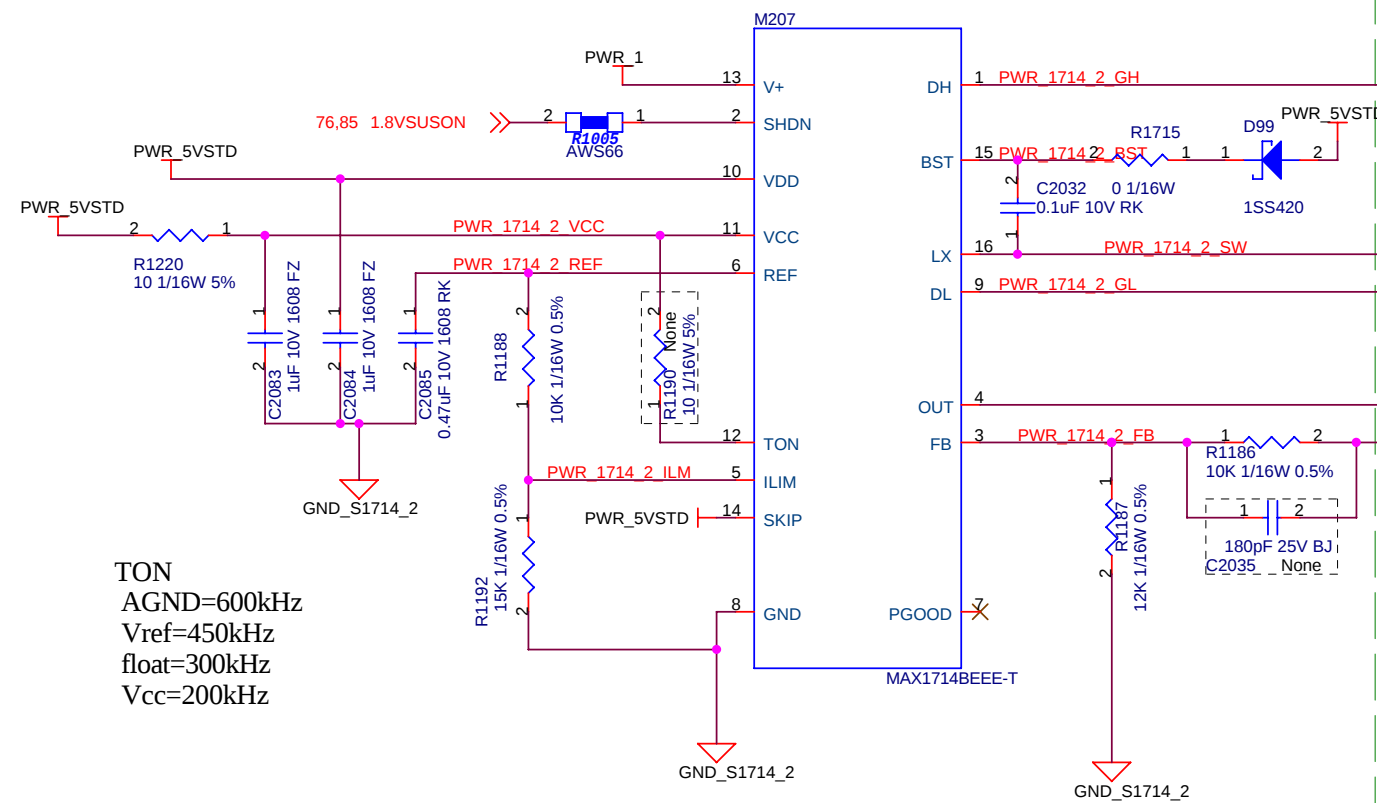


						TITLE VB313AA					
									DRAW. No. C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description				Sheet 79 / 93		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa				
FUJITSU LTD.											



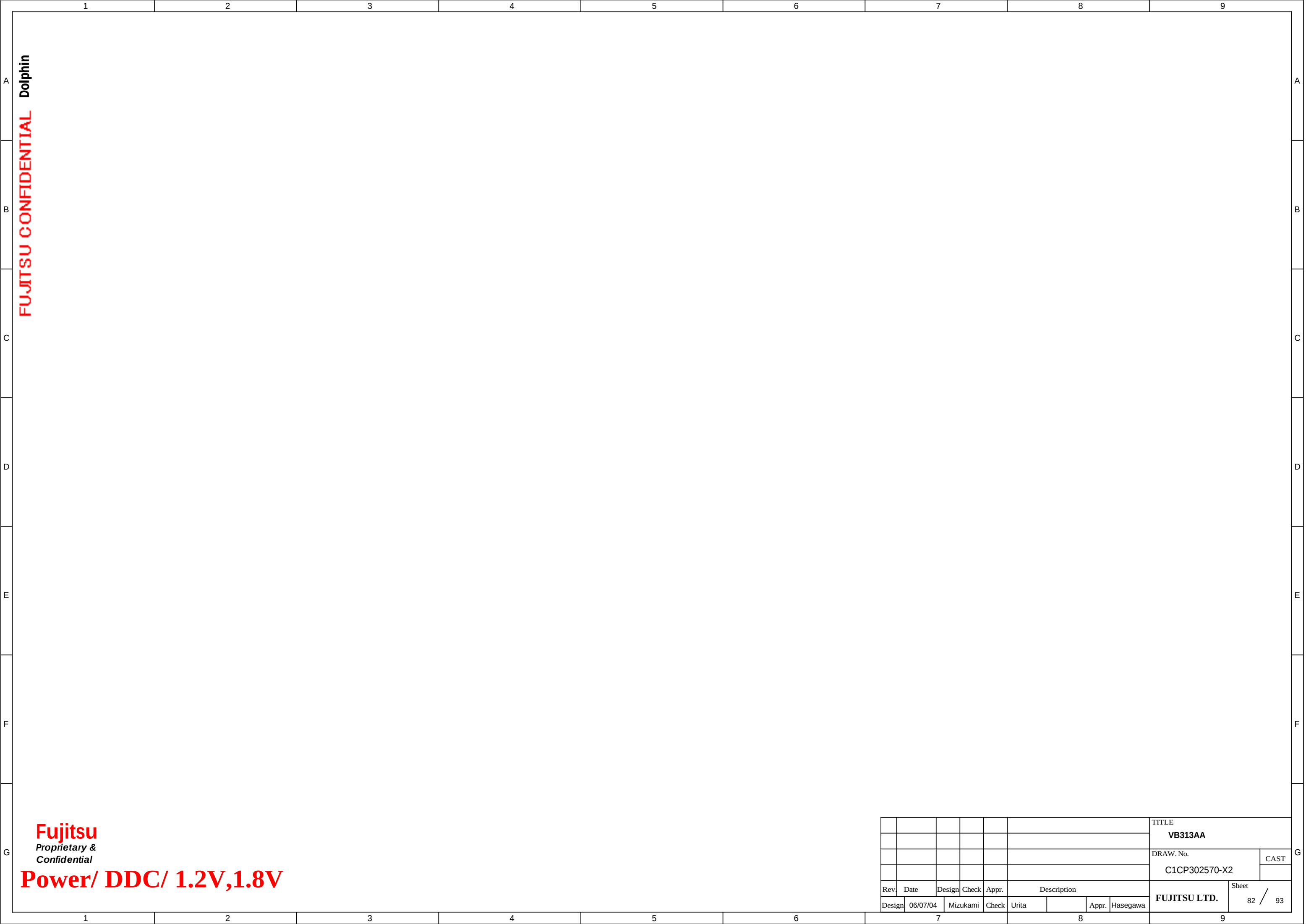
Power/ DDC/ 1.2VMAIN

									TITLE VB313AA	
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									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				FUJITSU LTD.	Sheet 80 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa			



Power/ DDC/ 1.8VSus

						TITLE VB313AA DRAW. No. C1CP302570-X2 CAST			
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		81 / 93



FUJITSU CONFIDENTIAL

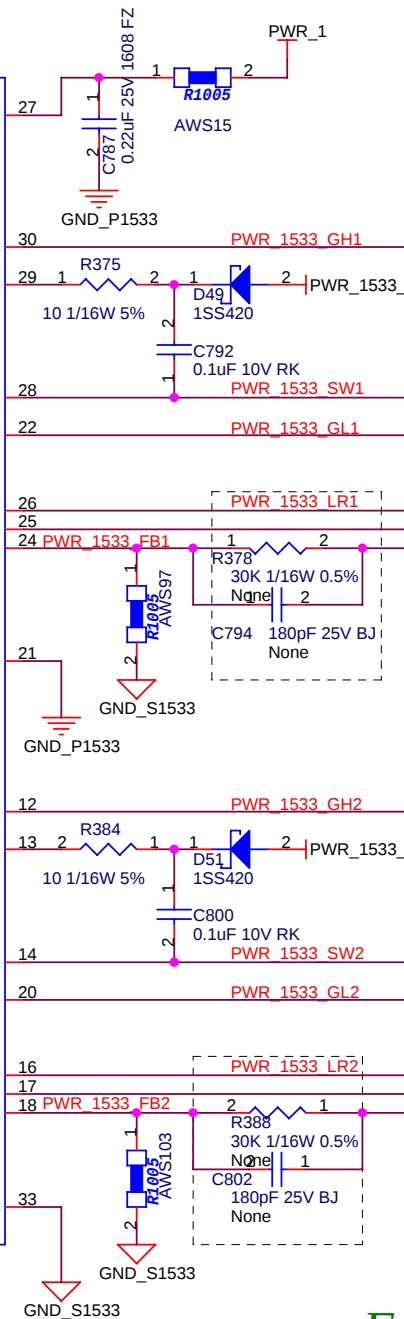
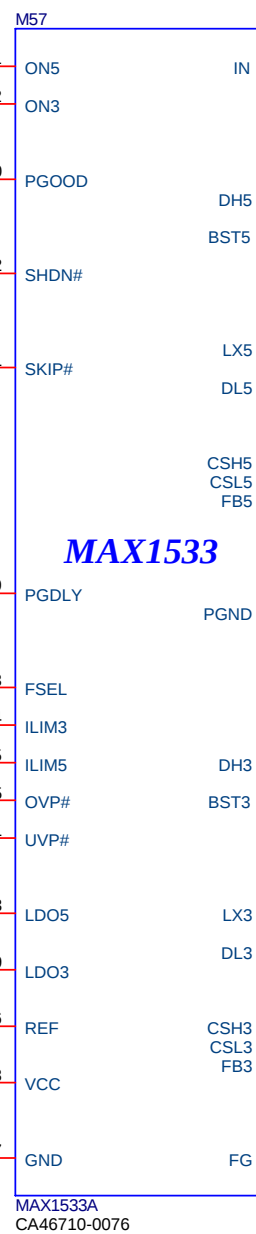
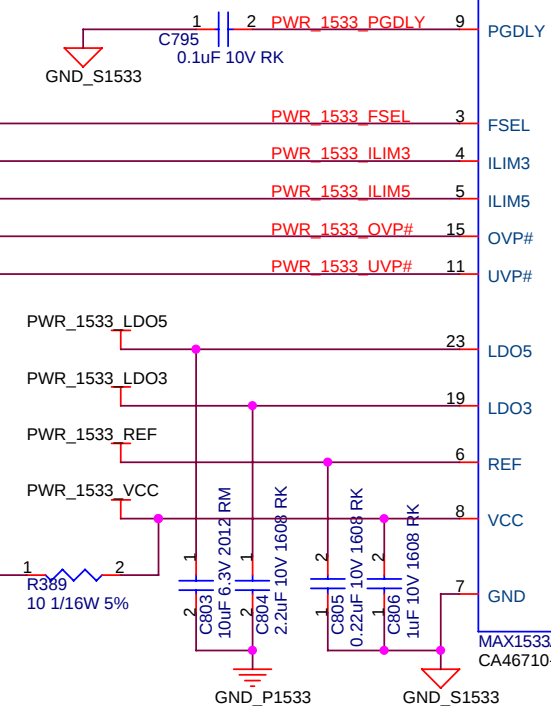
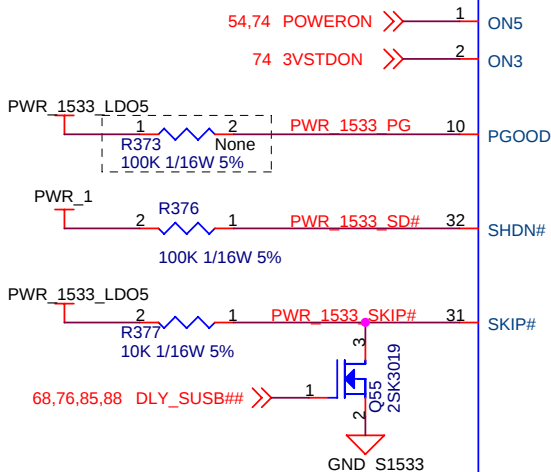
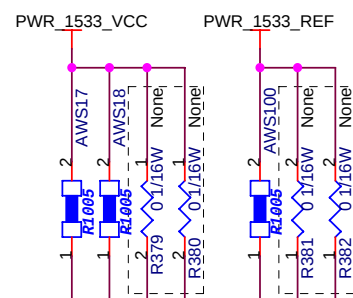
Dolphin

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Power/ DDC/ 1.2V,1.8V

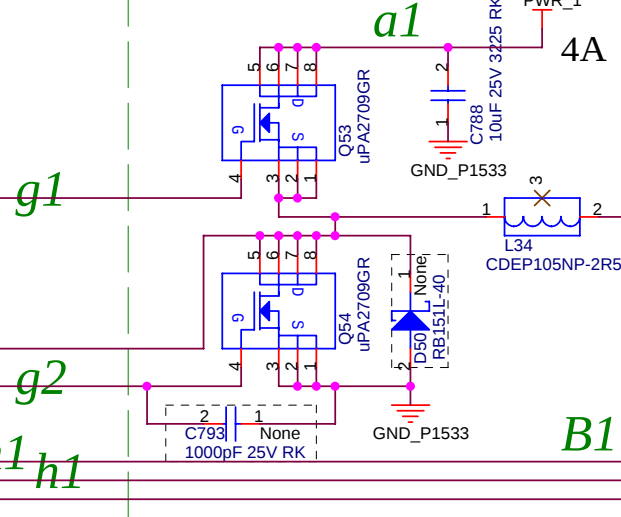
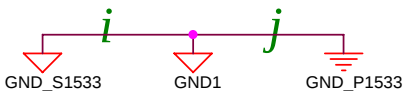
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						VB313AA			
						DRAW. No.			CAST
						C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.		Sheet
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Frequency Select: FSEL(3pin)
VCC=500kHz
REF=300kHz
GND=200kHz
I Limit: ILIM(4,5pin)
VCC=75mV
or
V(ILIM)/10 V
(50mV-200mV)

Under/Over Voltage Protection:
OVP#(15pin)/UVP#(11pin)
H=disable
L=enable

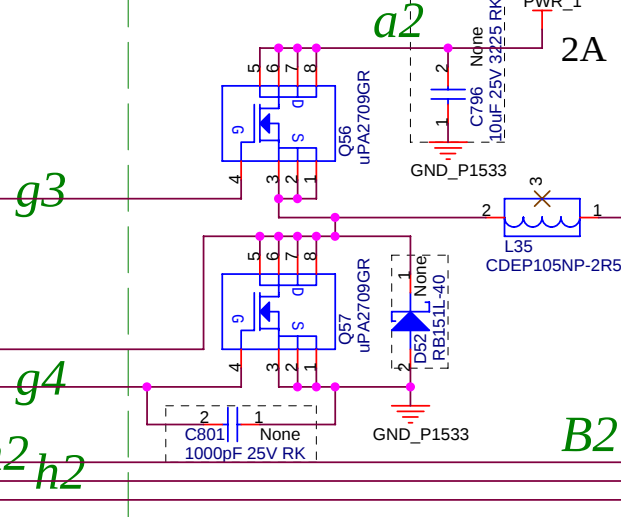


F



B1

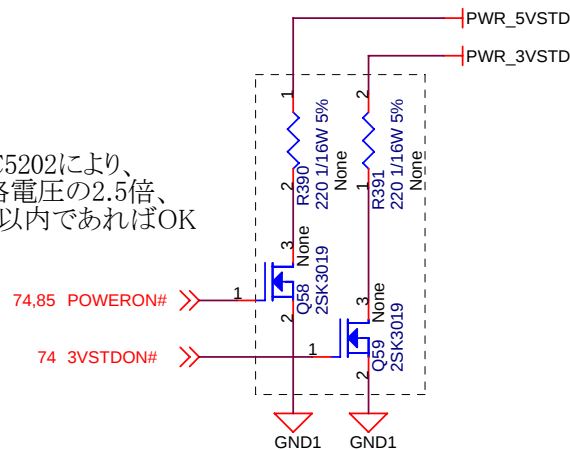
C1



B2

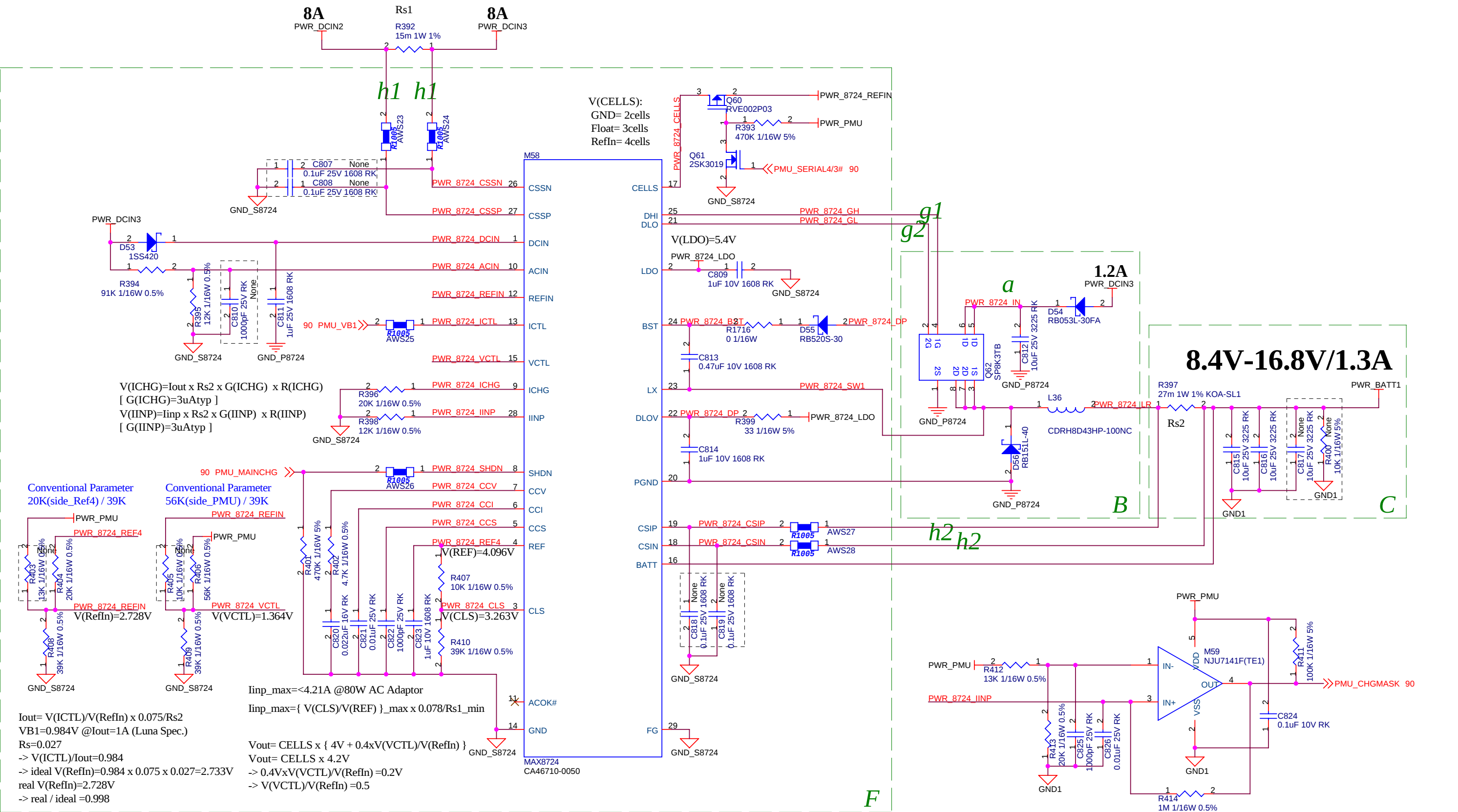
C2

JISC5202により、
定格電圧の2.5倍、
5秒以内であればOK

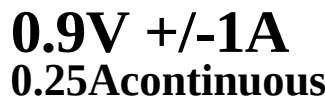


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Power/ DDC/ 3.3V,5V

								TITLE	
								VB313AA	
								DRAW.No.	CAST
								C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet
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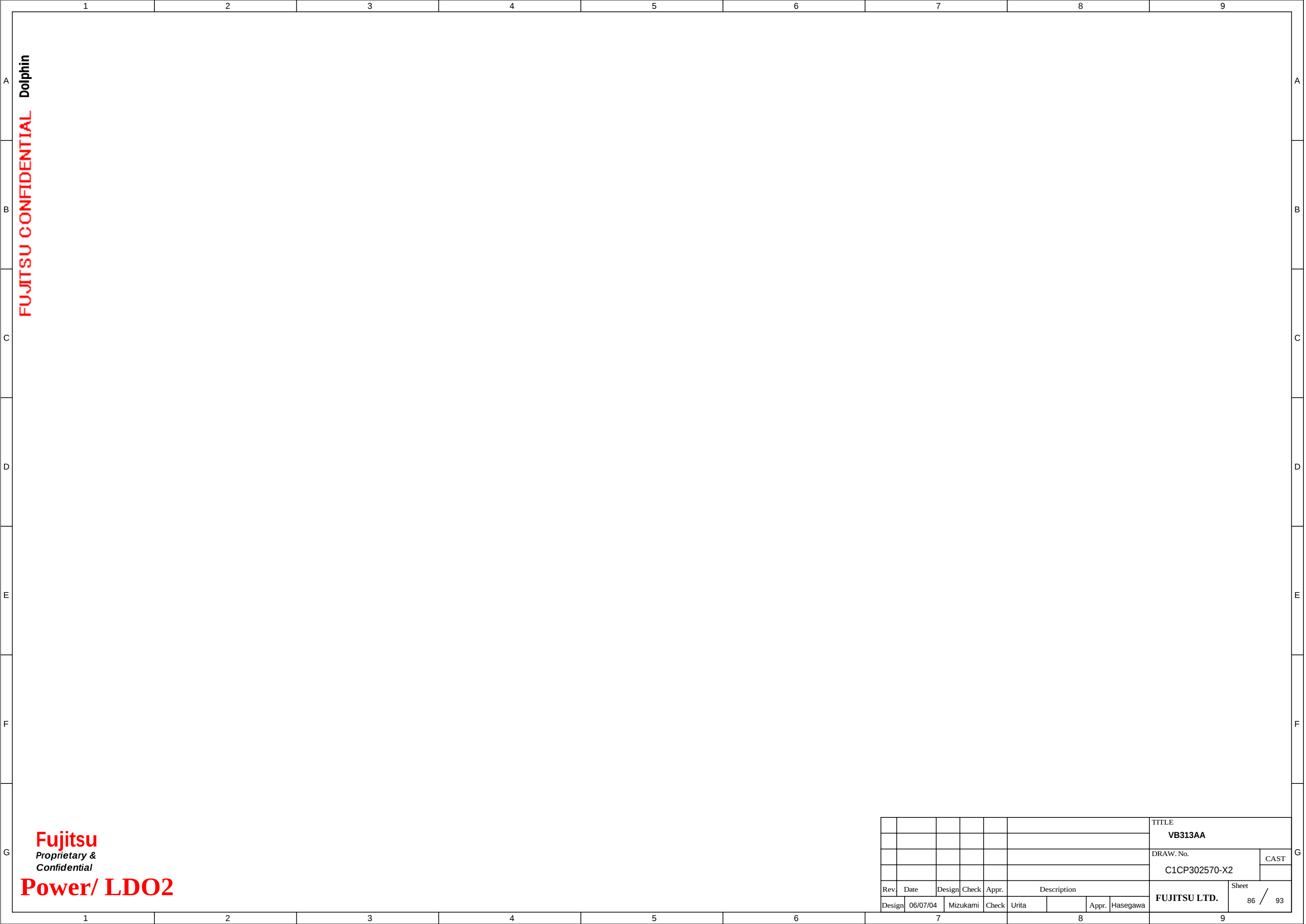


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Rev.	Date	Design	Check	Appr.	Description		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa
					FUJITSU LTD.		Sheet 84 / 93



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									TITLE	
									VB313AA	
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									CAST	
									C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description				Sheet	
Design	06/07/04	Mizukami	Check	Urita			Appr.	Hasegawa	FUJITSU LTD. 85 / 93	



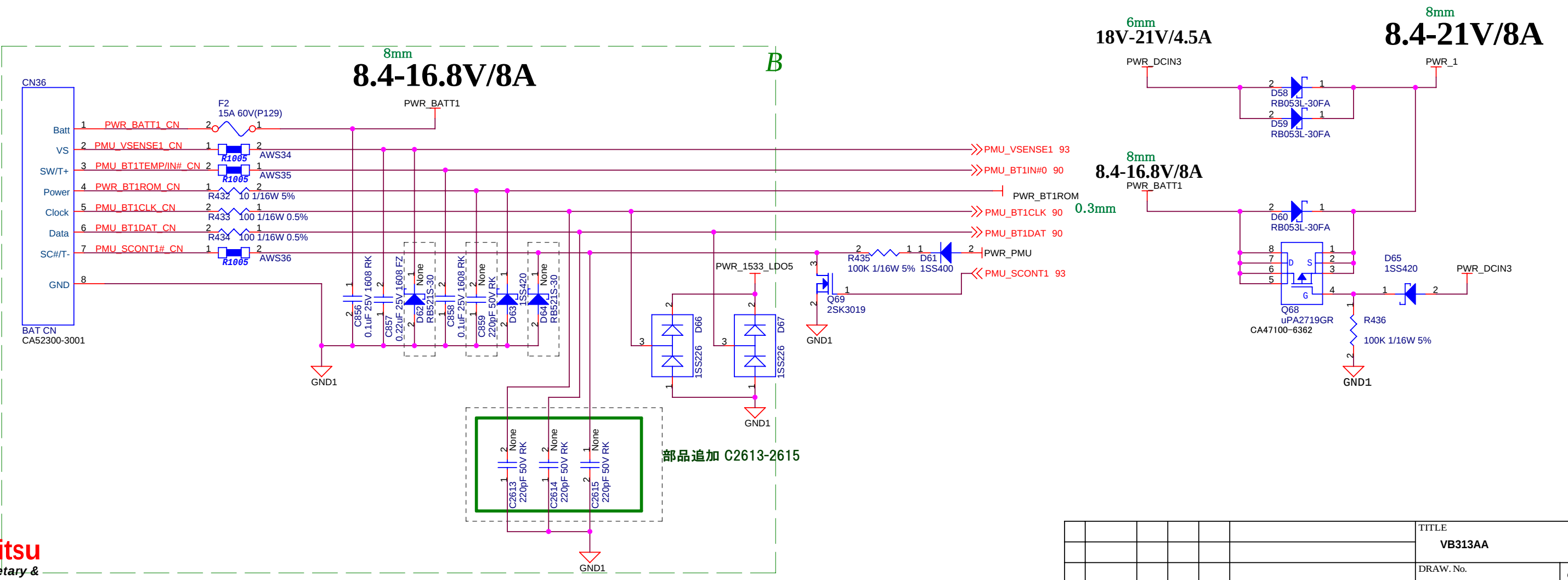
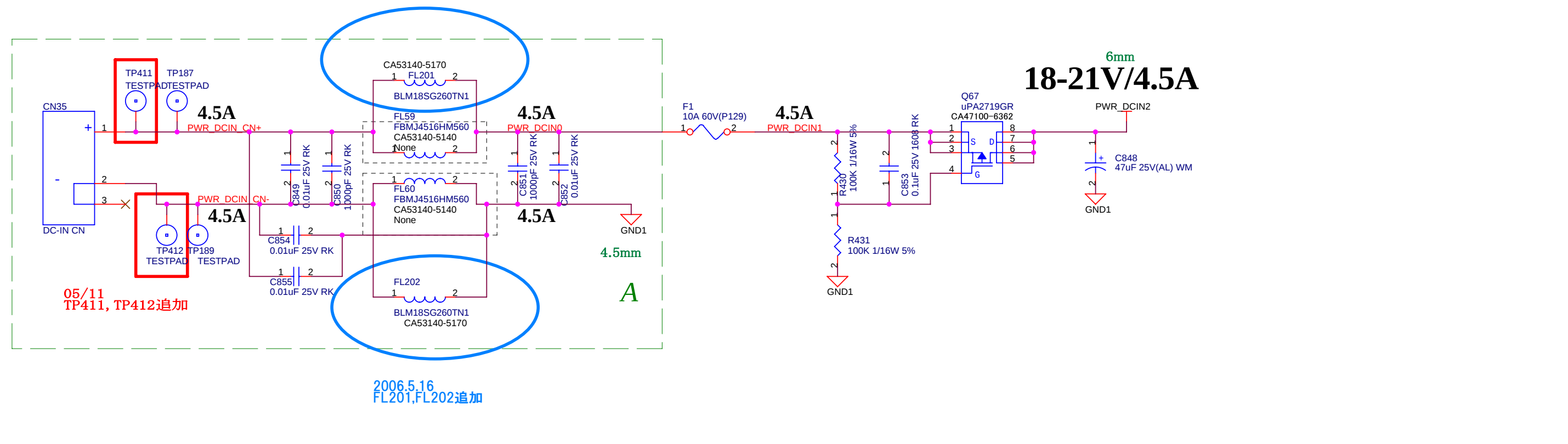
FUJITSU CONFIDENTIAL

Dolphin

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Power/ LDO2

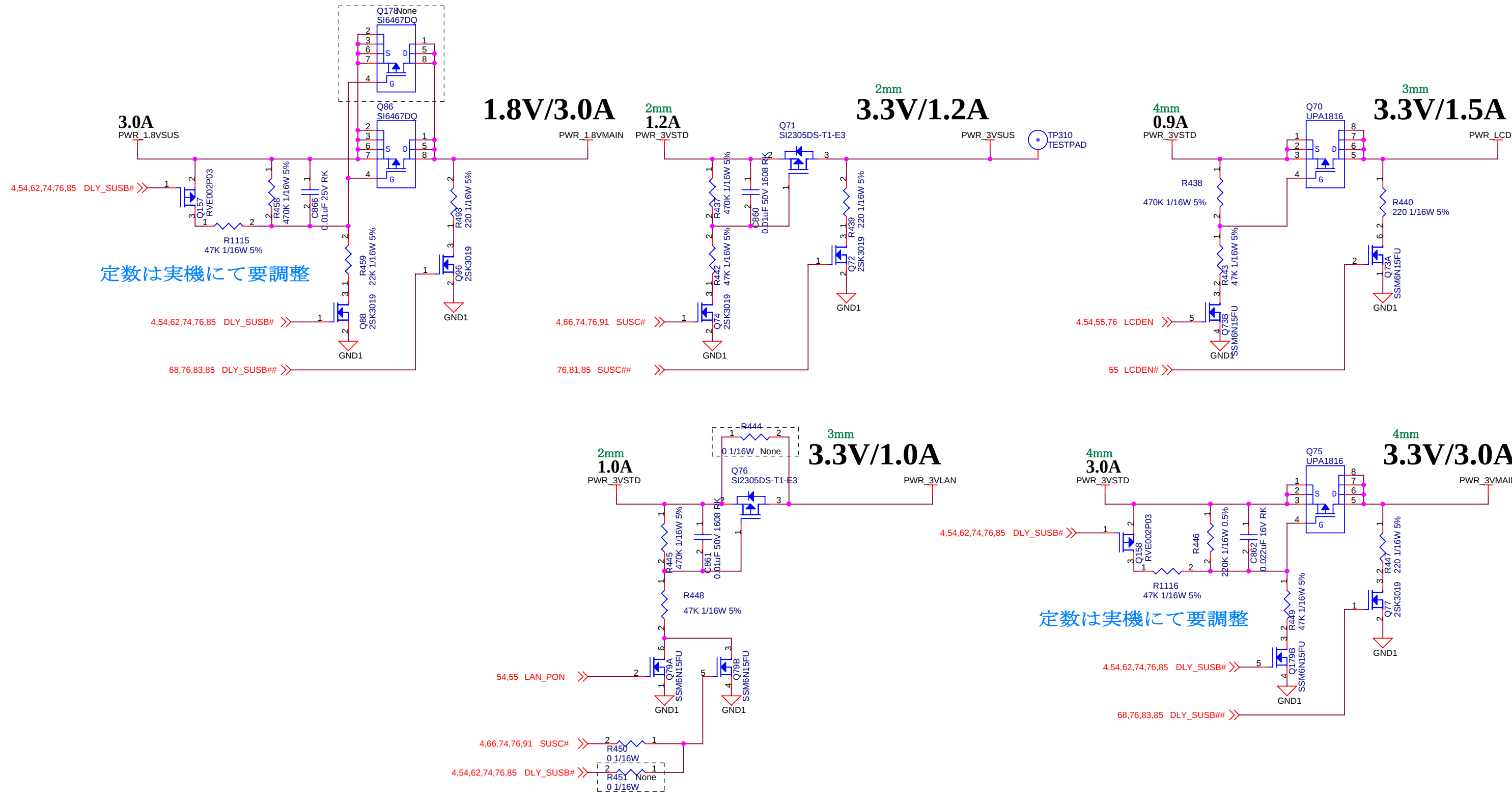
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Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.		Sheet
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	86 /	93

ゴミ信号線削除

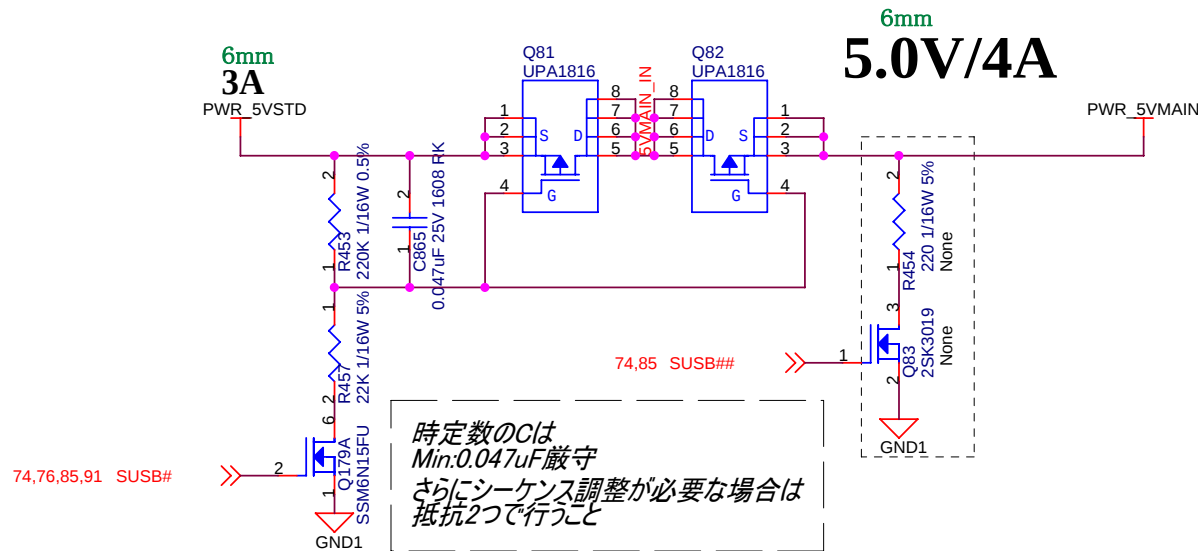
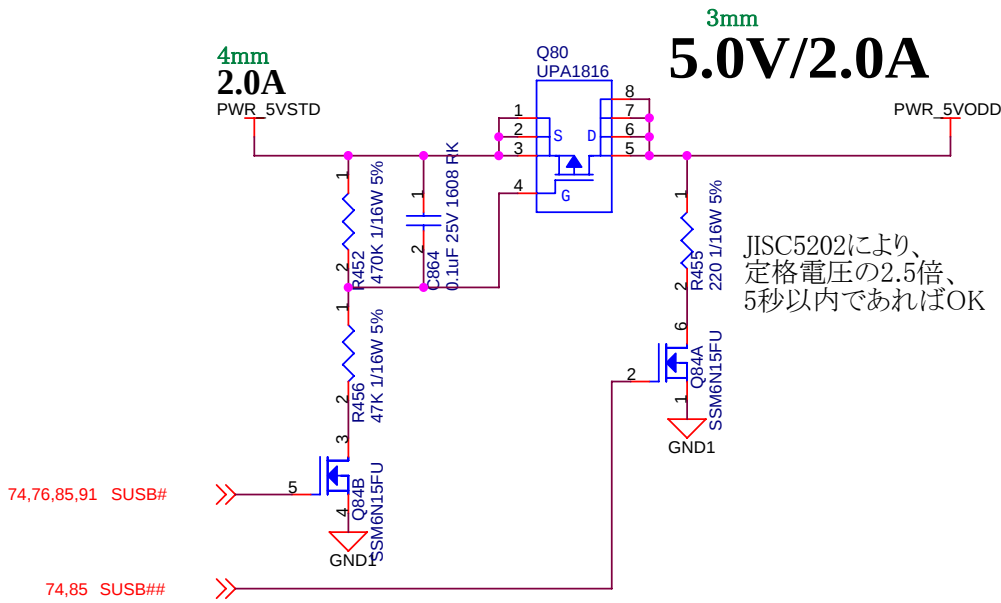


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Power/ Node/ DCIn, Battery CN

					TITLE			
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Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa	FUJITSU LTD.	
							87 / 93	

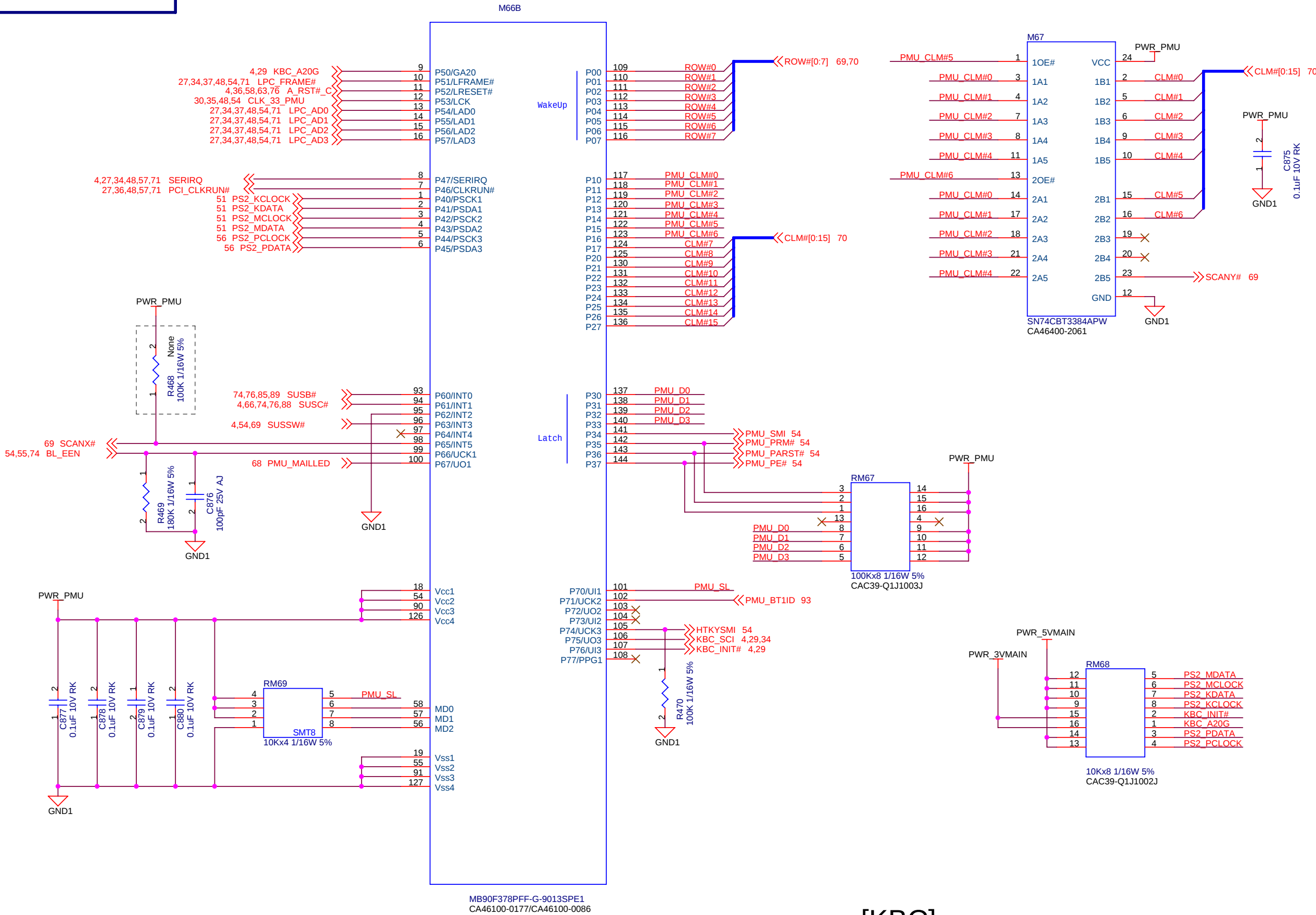
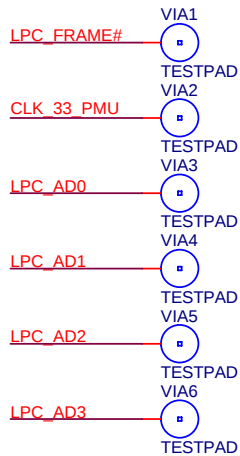


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Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita		88	93
						FUJITSU LTD.	



						TITLE		
						VB313AA		
						DRAW. No.		CAST
						C1CP302570-X2		
Rev.	Date	Design	Check	Appr.	Description			Sheet
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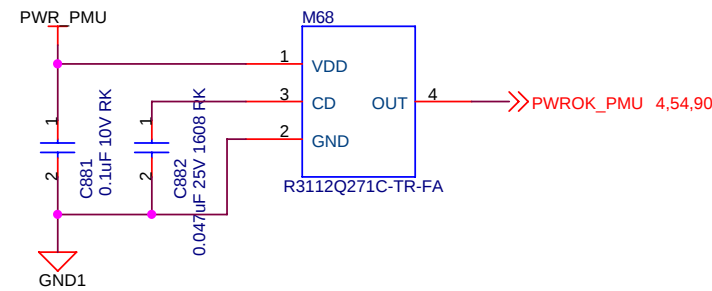
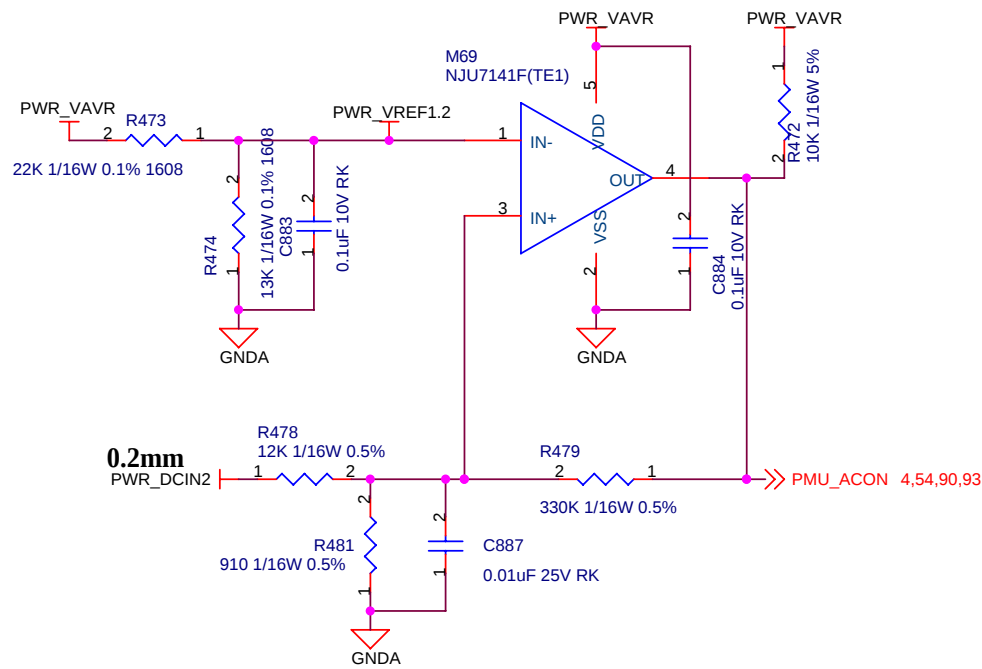
本ページで追加したVIAはTPとして使用する。
シルクを入れること。



本ページの抵抗・コンデンサはM38867付近に配置すること。
パソコンについてはM38867の電源ピンに対して均等になるように配置分散し、
電源ピンまでのリード長を最大限短くなるようレイアウトすること。

[KBC]

					TITLE			
					VB313AA			
					DRAW. No.		CAST	
					C1CP302570-X2			
Rev.	Date	Design	Check	Appr.	Description		Sheet	
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Target 200ms
遅延ターゲット
R3112N271C-TR:
 $T_{plh}(s) = 0.69(TYP) \times 6.5(M\Omega) \times CT(F)$

A

LUNA近傍に配置

						TITLE	
						VB313AA	
						DRAW. No.	CAST
						C1CP302570-X2	
Rev.	Date	Design	Check	Appr.	Description	Sheet	
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa
FUJITSU LTD.						92 /	93

